CoreModule® 920
Single Board Computer
Reference Manual

P/N 50-1Z144-1000

Notice Page

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Chapter 1 About This Manual

Purpose of this Manual

This manual is for designers of systems based on the CoreModule® 920 Single Board Computer (SBC). This manual contains information that permits designers to create an embedded system based on specific design requirements.

Information provided in this reference manual includes:

- Product Overview
- Hardware Specifications
- BIOS Setup information
- Technical Support Contact Information

Information not provided in this reference manual includes:

- Detailed chip specifications (refer to the References section of this chapter)
- Internal component operation
- Internal registers or signal operations
- Bus or signal timing for industry-standard busses and signals
- Pin-signal definitions for industry-standard interfaces

References

The following list of references may help you successfully complete your custom design.

Industry Standard Specifications

- PCI/104-Express Specification, Revision 2.0, February, 2011

  Web site: http://www.pc104.org/pci104_Express_specs.php
- PCI-104 Specification

  Web site: http://www.pc104.org/pci_104_specs.php
- PCI Express Specification, Revision 2.0, January, 2007

  Specification (for members): http://www.pcisig.com/specifications/pciexpress/base2/#b21
- PCI Specification, Revision 2.3, March 29, 2002

  Web site: http://www.pcisig.com
- LPC Specification Version 1.1

  Web site: http://www.intel.com/design/chipsets/industry/lpc.htm
- USB Specification Version 2.0

  Web site: http://www.usb.org/developers
- SATA Specification Version 3.0

  Web site: http://www.sata-io.org/
- Ethernet IEEE802.3 Specifications

  Web site: http://standards.ieee.org/about/get/802/802.3.html

- SMBus Specification Version 2.0

  Specification: http://smbus.org/specs/

- AMI BIOS Aptio TSE User's Guide

  Data sheet: http://www.ami.com/support/doc/AMI_TSE_User_Manual_PUB.pdf

Chip Specifications

The following integrated circuits (ICs) are used in the CoreModule 920 SBC.

- Intel® Corporation and the Mobile 3rd Generation Core™i7 CPU integrated processor core and graphics memory hub

  Web site: http://www.intel.com/p/en_US/embedded/hwsw/hardware/core-hm76/hardware

- Hynix Semiconductor, Inc. and the H5TQ2G83BFR-H9, DDR3 on-board System SDRAM

  Web site: http://www.hynix.com/gl/products/consumer/consumer_info.jsp

- Intel Corporation and the BD82QM67, 6 Series Express chipset, featured as the Platform Controller Hub (PCH)

  Datasheet: http://www.intel.com/Assets/PDF/datasheet/324645.pdf

- Intel Corporation and the 82574IT, Gigabit Ethernet controller

  Data sheet: http://download.intel.com/design/network/datashts/82574.pdf

- Intel Corporation and the 82579LM, Gigabit Ethernet PHY (physical layer) transceiver

  Data sheet: http://www.intel.com/content/www/us/en/ethernet-controllers/ethernet-controllers.html

- Atmel Corporation and the AT25128B-SSHL-B, Ethernet EEPROM

  Data sheet: http://www.atmel.com/dyn/resources/prod_documents/doc8535.pdf

- Fintek, Inc. and the F81216AU-I, LPC to 4 UART Controller

  Data sheet: http://www.fintek.com.tw/files/productfiles/F81216_V032P.pdf

- Texas Instruments and the XIO2001IPNP, PCIe-to-PCI bridge

  Web site:

  http://www.ti.com/sitesearch/docs/universalsearch.tsp?searchTerm=XIO2001IPNP&linkId=1

- Texas Instruments and the TR3253EIRSMR RS-232, serial transceiver

  Web site: http://www.ti.com/lit/ds/slls850b/slls850b.pdf

- Greenliant and the GLS85LS1008P Solid State NANdrive

  Data sheet: http://www.greenliant.com/products/solid_state_storage.dot#sn

- ON Semiconductor and the ADT7490-D, Hardware Monitor

  Data sheet: http://www.onsemi.com/pub_link/Collateral/ADT7490-D.PDF

- Winbond Corporation and the W25Q64BVSSIG SPI Flash BIOS chip

  Web site: http://www.winbond.com/hq/enu

- ST Microelectronics and the STHDLS101TQTR, HDMI Level Shifter

  Web site: http://www.st.com/internet/com/home/home.jsp

- Atmel Corporation and the AT24C02C for SPD and PCIe-to-PCI Bridge EEPROMs

  Web site: http://www.atmel.com/devices/at24c02c.aspx?tab=documents

- Wurth Elektronik Company and the 7490200110, Gigabit Ethernet Transformers

  Data Sheet: http://katalog.we-online.de/pbs/datasheet/749020011.pdf

NOTE If you are unable to locate the datasheets using the links provided, search the internet using the name of the manufacturer or component model and locate the documents you need.

Chapter 2 Product Overview

This overview presents general information about the PCI/104-Express form factor and the CoreModule 920 Single Board Computer (SBC). After reading this chapter you should understand the following points with regard to the CoreModule 920.

- PCI/104-Express From Factor
- Product Description
- Major Components (ICs)
- Headers, Connectors, and Sockets
- Product Specifications

PCI/104-Express Form Factor

This product is based on PCI Express architecture and the PCI/104-Express form factor. The PCI/104-Express form factor affords a great deal of flexibility in system design. You can build a simple system using only a CoreModule SBC, input/output devices connected to serial, USB, or SATA ports, and the on-board storage device. To expand a simple CoreModule system, simply add self-stacking expansion modules to provide additional capabilities, such as:

- Additional serial and parallel ports
- Analog or high-speed digital I/O
    - Data Acquisition (Analog In/Out)
    - USB 2.0 expansion modules
    - IEEE 1394 (FireWire) expansion modules
    - Standard VGA video output

PCI/104-Express-compliant expansion modules can be stacked with a CoreModule SBC, avoiding the need for large, expensive card cages and backplanes. These expansion modules can be mounted directly to the expansion connectors of the CoreModule, with inter-board spacings of ~0.6 inches, so that a 3-module system fits in a 4.6" x 3.8" x 2.0" space. See Figure 2-1.

One or more PCI/104-Express-compliant modules can be installed on the CoreModule SBC expansion connectors so that the expansion modules fit within the CoreModule outline dimensions. The PCI/104-Express form factor allows for several modules to be stacked up or down from the CoreModule expansion connectors with each additional module increasing the thickness of the package by ~17mm (0.6"). See Figure 2-1.

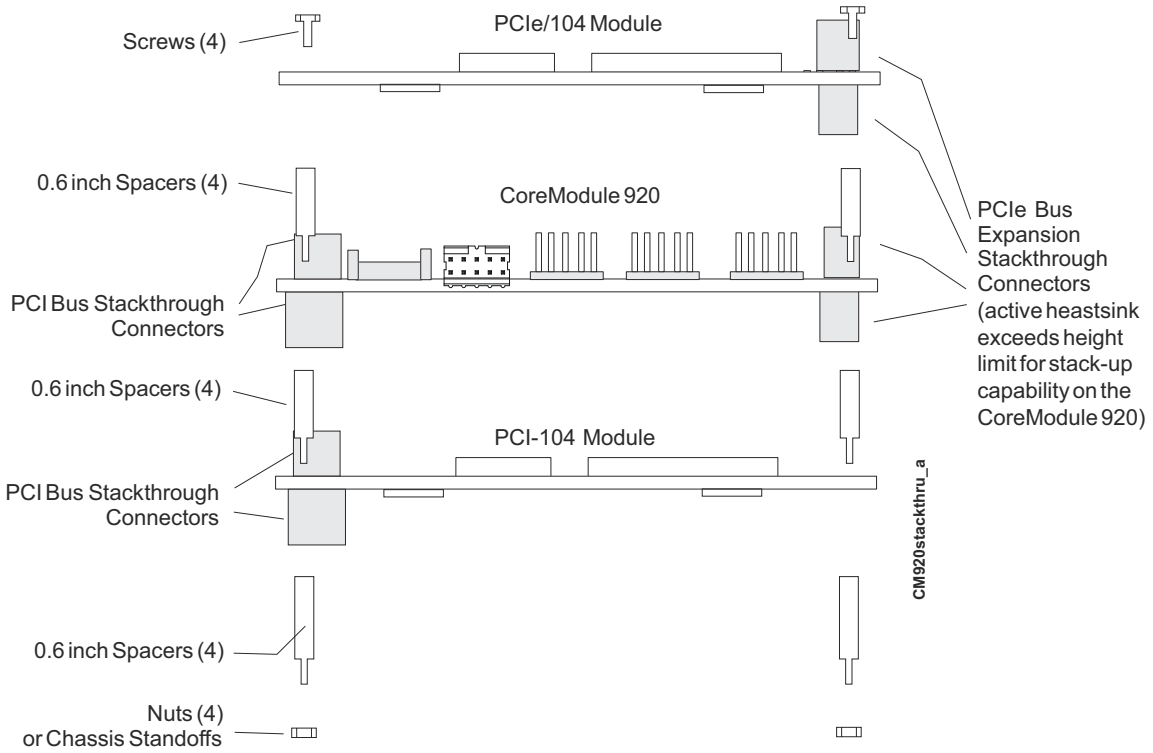

Figure 2-1. Stacking PCI/104-Express Modules with the CoreModule 920

Product Description

The CoreModule 920 SBC is a highly integrated, high-performance, Intel® Core™ i7 processor based system, compliant with PCI Express architecture and the PCI/104-Express form factor. This rugged and high quality single-board system contains all the component subsystems of an ATX motherboard, plus the equivalent of several PCI and PCI Express expansion boards.

The Intel Core i7 series CPU integrates a multiple execution core with a Graphics and Memory Controller Hub (GMCH), providing a high-performance processor, a memory controller for up to 2GB of DDR3 on-board memory, and a graphics controller that provides VGA, LVDS, and HDMI ports driven by the PCH (Platform Controller Hub) and one PCIe x16 Graphics (PEG) port driven by the CPU.

Each CoreModule 920 incorporates an Intel BD82QM67 PCH, providing the controller hub for a range of common user interfaces including six USB 2.0 ports, two serial ports, two SATA 3.0 ports, one SATA 2.0 port dedicated for the SSD, four PCIe x1 lanes, as well as interfaces for GPIO and RTC battery. The CoreModule 920 provides a Solid State Drive through the SATA2 port for storage up to 8GB, a Hardware Monitor chip to control temperature and voltage levels, and a Utility interface for Power button, Reset switch, and Speaker output. The PCH connects to two 10-pin Gigabit Ethernet interfaces through two PCIe x1 lanes.

The CoreModule 920 can be expanded through the PCIe expansion bus using the PCI-104 and PCIe/104 interfaces for additional system functions. These interfaces offer compact, self-stacking, modular expandability. The PCI-104 interface implements a PCI bus available on a 120-pin (4 rows of 30 pins) PCI expansion bus connector. The PCIe/104 interface includes the PCIe signal set plus SMBus and USB 2.0 signals available on top and bottom-side, 156-pin high-speed PCIe connectors. The PCI bus operates at a clock speed of up to 33MHz, and the PCIe bus operates at a clock speed of up to 100MHz.

The CoreModule 920 is particularly well suited to either embedded or portable applications and meets the size, power consumption, temperature range, quality, and reliability demands of embedded system applications. It can be stacked with ADLINK expansion modules or other PCI/104-Express-compliant expansion modules, or it can be used as a powerful computing engine. The CoreModule 920 requires a single +5V AT power source.

Module Features

- CPU
  - Provides a 1.7GHz (17W) Intel Core i7 3517UE Processor Core and Graphics Memory Controller Hub
  - Provides a DMI (Direct Media Interface) with 2 GB/s of bandwidth in each direction
  - Provides an FDI (Flexible Display Interface) for carrying display traffic to the PCH
  - Provides Enhanced Intel SpeedStep® Technology (EIST)
  - Supports Hyper-Threading Technology
  - Provides up to 8MB on-die L3 cache
  - Provides 3D graphics engine
  - Provides dual-channel DDR3 memory controller (only one channel connected on board)
- Memory
  - Provides 2GB of +1.5V DDR3 soldered, on-board memory
  - Provides double data rate interface
  - Supports 32-bit data bus
  - Supports DDR3 1333MHz memory
- Expansion Buses
  - PCI bus version 2.3 at 33MHz
  - PCIe bus version 2.0 at 100MHz
- SATA Interface
  - Supports two SATA 3.0 ports from the BD82QM67 PCH
  - Supports up to 6Gb/second data transfer rate
  - Supports independent DMA operation
  - Supports Native Command Queuing
  - Provides Auto Activate for DMA
  - Supports Hot Plug features
  - Provides two standard SATA 3.0 connectors
  - Supports one SATA 2.0 port dedicated for the SSD (Solid State Drive)
- Serial Interface
  - Provides two buffered serial ports (COM1-2) with full handshaking
  - Provides two 10-pin headers
  - Provides 16550-equivalent controllers with 16-byte FIFO modes
  - Supports full-duplex buffering and full status reporting
  - Supports full modem capability
  - Supports programmable word length, stop bits, and parity
  - Provides programmable baud-rate generator

- USB 2.0 Interface
  - Provides two root USB 2.0 hubs
  - Provides up to six USB 2.0 ports
  - Supports USB bootable devices
  - Supports USB Keyboard and Mouse
  - Supports USB v2.0 EHCI and v1.1 UHCI
  - Supports over-current detection status
- Ethernet Interface
  - Provides two fully independent Gigabit Ethernet ports
  - Provides integrated LEDs on each port (Link/Activity and Speed)
  - Provides one Intel 82574IT controller chip and one 82579LM PHY transceiver chip
  - Provides two 10-pin headers for Gigabit Ethernet user interface
  - Provides two headers for GLAN LED signals
  - Supports IEEE 802.3 10/100BaseT and 10/100/1000BaseT compatible physical layers
  - Supports Auto-negotiation for speed, duplex mode, and flow control
  - Supports full-duplex or half-duplex mode
    - Full-duplex mode supports transmit and receive frames simultaneously
    - Supports IEEE 802.3x Flow control in full-duplex mode
    - Half-duplex mode supports enhanced proprietary collision reduction mode
- Video Interfaces (VGA, HDMI, LVDS, and PEG)
  - Provide VGA outputs
    - Resolutions up to 2048x1536 pixels at 75Hz
    - Integrated 340.4MHz RAMDAC with 32-bit color
    - RGB output provided by three 8-bit DACs
    - HSYNC and VSYNC output
  - Provide HDMI outputs
    - Resolutions up to 3840x2160 pixels at 30Hz
    - Pixel clock rates from 25MHz to 340MHz
    - Support for DVD-Audio and Audio Return Channel
  - Provide LVDS flat panel outputs
    - Single channel capability
    - Resolutions up to 1400x1050 at 60Hz
    - Pixel clock rates of 25MHz to 112MHz
    - Pixel color depths of 18 and 24 bits
  - Support PCI Express graphics (PEG)
    - External high-performance PCI Express graphics cards
    - General-purpose PCI Express devices
    - Theoretical bandwidth of up to 8GT/s
    - PCIe Gen3 compliance

- GPIO Interface
  - Provides two 6-pin interface headers
  - Supports a total of eight GPIO ports
  - Supports sample code in BSP QuickDrive
- Utility Interface
  - Power Button
  - Reset Switch
  - Speaker
- Miscellaneous
  - Real Time Clock (RTC) with external replaceable battery
  - Battery-free boot
  - Oops! Jumper support
  - Serial Console support
  - Watchdog Timer
  - Logo Screen (Splash)
  - SSD (Solid State Drive)
  - Hardware Monitor (voltage and temperature)

Block Diagram

Figure 2-2 presents a functional representation of the CoreModule 920.

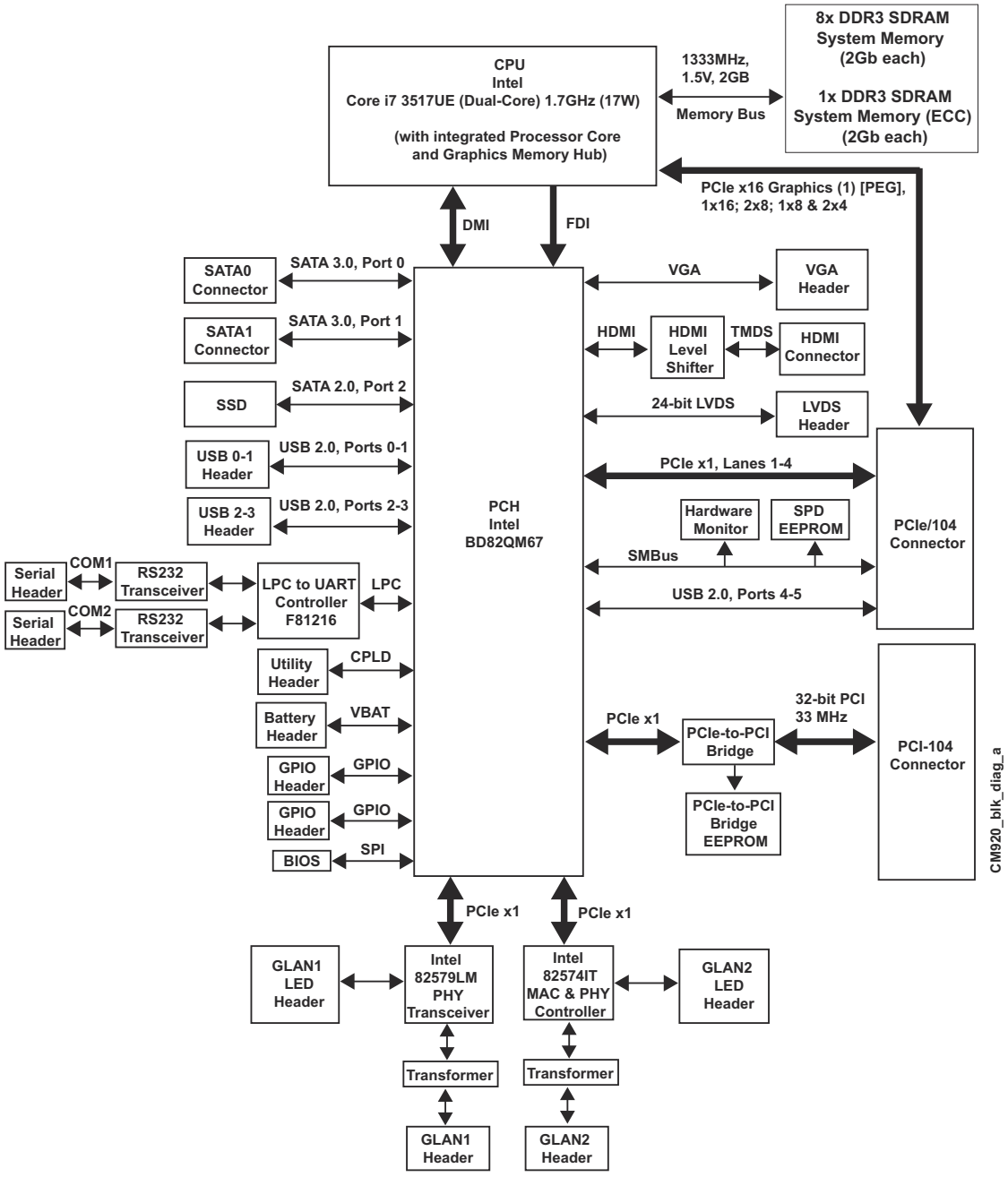

Figure 2-2. Functional Block Diagram

Major Component (ICs) Definitions

Table 2-1 lists the major ICs, including a brief description of each, on the CoreModule 920. Figures 2-3 and 2-4 show the locations of the major ICs.

Table 2-1. Major Component Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	Core™ i7, 3517UE, 1.7GHz (17W)	Central Processing Unit with 2 execution cores and up to 8MB L3 cache	Integrates Processor Core and Graphics Memory Controller Hub
DDR3 SDRAM (U3, U5, U8, U10, U11 [to enable ECC])	Hynix	H5TQ2G83BFR-H9	On-board DDR3 256M x 8 System Memory	Provides high-speed data transfer
DDR3 SDRAM (U4, U6, U7, U9 - on bottom side [see Figure 2-4])	Hynix	H5TQ2G83BFR-H9	On-board DDR3 256M x 8 System Memory	Provides high-speed data transfer
PCH [Platform Controller Hub (U12)]	Intel	BD82QM67 (PCH)	I/O Hub for common user interfaces	Provides Southbridge interfaces and off loads some Northbridge functions from the CPU
Gigabit Ethernet PHY Transceiver (U14)	Intel	82579LM	Single-port Gigabit Ethernet PHY Transceiver for GLAN1 interface	Provides a standard IEEE 802.3 Ethernet interface for Ethernet transfer rates up to 1000 Mb/s
Gigabit Ethernet Controller (U15)	Intel	82574IT	Gigabit Ethernet controller for GLAN2 interface	Generates PCIe 10T/100TX/ 1000T Ethernet signals
Ethernet EEPROM (U16)	Atmel	AT25128B-SSHL-B	Three-Wire Serial EEPROM for Gigabit Ethernet Controller	Provides storage for MAC addresses, serial numbers, and pre-boot configuration data
PCIe-to-PCI Bridge (U17)	Texas Instruments	XIO2001IPNP	PCIe-to-PCI interface	Migrates legacy PCI interfaces
LPC-to-UART Controller (U18)	Fintek	F81216AU-I	Serial communication controller	Provides 4 UART ports through the LPC bus

Table 2-1. Major Component Descriptions and Functions (Continued)

RS-232 Transceiver (U20)	Texas Instruments	TR3253EIRSMR	Transceiver for Serial 1 RS-232 signals	Transmits and receives RS-232 signals for COM1
RS-232 Transceiver (U21)	Texas Instruments	TR3253EIRSMR	Transceiver for Serial 2 RS-232 signals	Transmits and receives RS-232 signals for COM2
Solid State Drive [SSD] - SATA (U22) - on bottom side [see Figure 2-4])	Greenliant	GLS85LS1008P	Industrial-grade soldered solid-state storage module	Provides solid state storage through SATA port 2
Hardware Monitor (U27) [on bottom side; see Figure 2-4]	ON Semiconductor	ADT7490-D	Remote Voltage and Temperature Monitor and Fan Controller	Provides system thermal protection
SPI Flash (U28)	Winbond	W25Q64BVSSIG	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS in Flash Memory
HDMI Level Shifter (U48)	ST Microelectronics	STHDLS101TQTR	HDMI level-shift IC for HDMI video	Converts HDMI differential input from the PCH to TMDS differential output for the HDMI interface
EEPROM, DDR3 (U66 - on bottom side [see Figure 2-4])	Atmel	AT24C02C	Two-Wire Serial EEPROM for SPD (Serial Presence Detect)	Provides storage for System Memory configuration data
EEPROM, PCIe-to-PCI Bridge (U66 - on bottom side [see Figure 2-4])	Atmel	AT24C02C	Two-Wire Serial EEPROM for PCIe-to-PCI Bridge	Stores PCIe-to-PCI bridge configuration data
Transformer - Gigabit Ethernet (T1)	Wurth Elektronik	7490200110	Gigabit Ethernet Magnetics	Provides electrical isolation for Gigabit Ethernet PHY transceiver (GLAN1)
Transformer - Gigabit Ethernet (T2)	Wurth Elektronik	7490200110	Gigabit Ethernet Magnetics	Provides electrical isolation for Gigabit Ethernet controller (GLAN2)

Key:
U1 - CPU
U3 - DDR3 SDRAM
U5 - DDR3 SDRAM
U8 - DDR3 SDRAM
U10 - DDR3 SDRAM
U11 - DDR3 SDRAM (ECC)
U12 - PCH
U14 - Gigabit Ethernet PHY Transceiver
U15 - Gigabit Ethernet MAC & PHY Controller
U16 - Gigabit Ethernet EEPROM
U17 - PCIe to PCI Bridge
U48 - HDMI Level Shifter

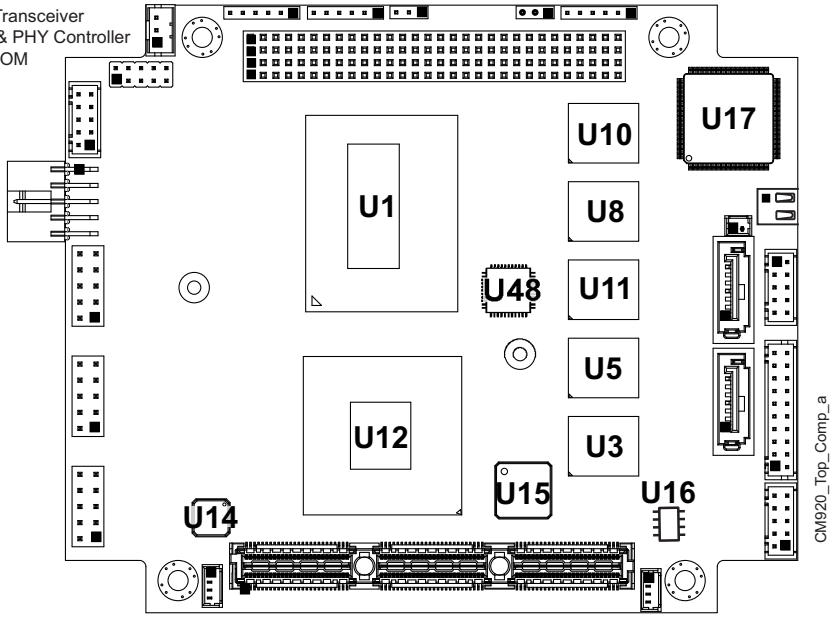

Figure 2-3. Component Locations (Top Side)

Key:
T1 - Gigabit Ethernet 1 Transformer
T2 - Gigabit Ethernet 2 Transformer
U4 - DDR3 SDRAM
U6 - DDR3 SDRAM
U7 - DDR3 SDRAM
U9 - DDR3 SDRAM
U18 - LPC to UART Controller
U20 - RS-232 Transceiver - COM1
U21 - RS-232 Transceiver - COM2
U22 - SSD (Solid State Drive)
U27 - Hardware Monitor
U28 - BIOS
U66 - EEPROM, DDR3 SPD
U67 - EEPROM, PCIe to PCI Bridge

J6 - PCI/104-Express
(See Header and Connector table)
SW1 - PCI Express x16 Configuration Switch
(See Header and Connector table)

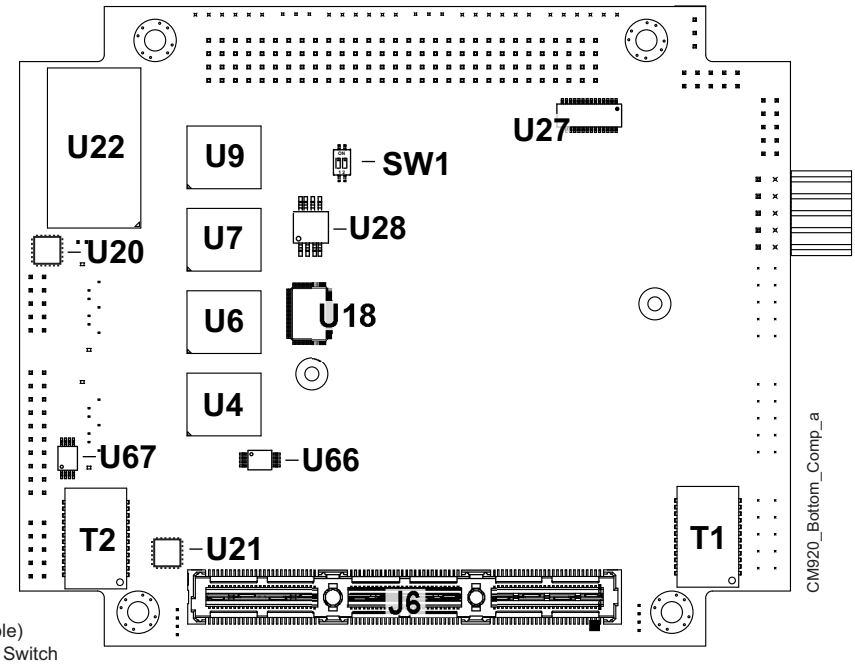

Figure 2-4. Component Locations (Bottom Side)

Header, Connector, and Socket Definitions

Table 2-2 describes the headers, connectors, and socket of the CoreModule 920 shown in Figure 2-6.

Table 2-2. Module Header and Connector Descriptions

Header #	Board Access	Description
H11 – GLAN1	Top	10-pin, 0.100" (2.54mm) header for Gigabit Ethernet port 1
H15 – USB (0-1)	Top	10-pin, 0.100" (2.54mm) header for USB 2.0 ports 0-1
H16 – COM2	Top	10-pin, 0.100" (2.54mm) header for serial port 2
J2 – LED - GLAN1	Top	4-pin, 0.049" (1.25mm) shrouded, single-row header for Gigabit Ethernet port 1 LED
J3 – LED - GLAN2	Top	4-pin, 0.049" (1.25mm) shrouded, single-row header for Gigabit Ethernet port 2 LED
J5 – PCIe/104	Top	156-pin, 0.025" (0.64mm) standard PCI Express connector for SMBus, USB 2.0, PCIe x1, and PCI interfaces
J6 – PCIe/104	Bottom	156-pin, 0.025" (0.64mm) standard PCI Express connector for SMBus, USB 2.0, PCIe x1, and PCI interfaces
J7 – PCI-104	Top/Bottom	120-pin, 0.079" (2mm) standard PCI-104 connector for PCI interfaces
J8 – HDMI (Micro)	Top	19-pin, 0.016" (0.04mm), standard micro-connector for HDMI video port
J10 – SATA0	Top	7-pin, 0.050" (1.27mm) standard connector for SATA 3.0 port 0
J12 – Battery	Top	2-pin, 0.049" (1.25mm) shrouded header for power from external battery
J13 – SATA1	Top	7-pin, 0.050" (1.27mm) standard connector for SATA 3.0 port 1
J14 – GLAN2	Top	10-pin, 0.079" (2mm) shrouded header for Gigabit Ethernet port 2
J17 – VGA	Top	10-pin, 0.079" (2mm) header for VGA video port
J18 – COM1	Top	10-pin, 0.079" (2mm) shrouded header for serial port 1
J21 – Utility	Top	6-pin, 0.079" (2mm) single-row header for Power Button, Reset Switch, and Speaker
J22 – Fan	Top	3-pin, 0.079" (2mm) shrouded header for power to external fan
J23 – LVDS	Top	20-pin, 0.079" (2mm) shrouded header for LVDS video port
J24 – Power	Top	10-pin, 0.100" (2.54mm) shrouded, right-angle header for supplying external power to the board
J25 – USB 2-3	Top	10-pin, 0.079" (2mm) shrouded header for USB 2.0 ports 2-3
J26 – GPIO1	Top	6-pin, 0.079" (2mm) single-row header for GPIO1

Table 2-2. Module Header and Connector Descriptions (Continued)

J27 – GPIO2	Top	6-pin, 0.079" (2mm) single-row header for GPIO2
SW1 – PCIe x16 Lane Configuration Switch (see Figure 2-4 on page 13.)	Bottom	4-pin dip switch for selecting CPU PCIe x16 lane configurations Switch Positions = Lane Configurations Pin 1, Pin 2 (off, off) = 1x8, 2x4 Pin 1, Pin 3 (off, on) = Reserved Pin 4, Pin 2 (on, off) = 2x8 Pin 4, Pin 3 (on, on) = 1x16 [Default] Switch Positions Pin 3 Pin 4 ON 1 2 Pin 2 Pin 1

NOTE The pinout tables in Chapter 3 of this manual identify pin sequence using the following method: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as 10-pin, 2 rows, odd/even (1, 2). See Figure 2-5.

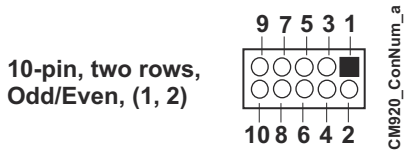

Figure 2-5. Connector Pin Sequence

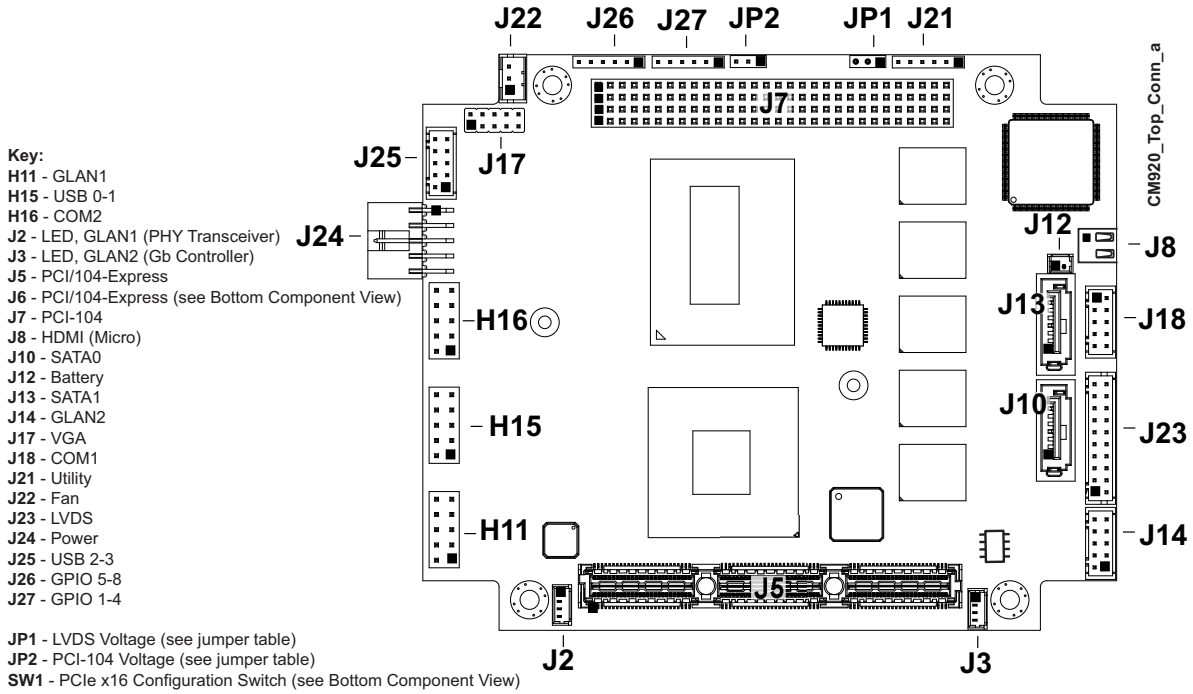

Figure 2-6. Header, Connector, and Socket Locations (Top Side)

NOTE	Black square pins on headers and connectors represent pin 1. Black square pins on right-angle headers represent pin 2.

Jumper Header Definitions

Table 2-3 describes the jumper headers shown in Figure 2-7. Both jumper headers provide 0.079" (2mm) pitch.

Table 2-3. Jumper Settings

Jumper Header	Installed	Moved
JP1 – LVDS Voltage Selection	Enable +3.3V (1-2) **(Default)**	Enable +5V (2-3)
JP2 – PCI-104 Voltage Selection	Enable +3.3V (1-2) **(Default)**	Enable +5V (2-3)

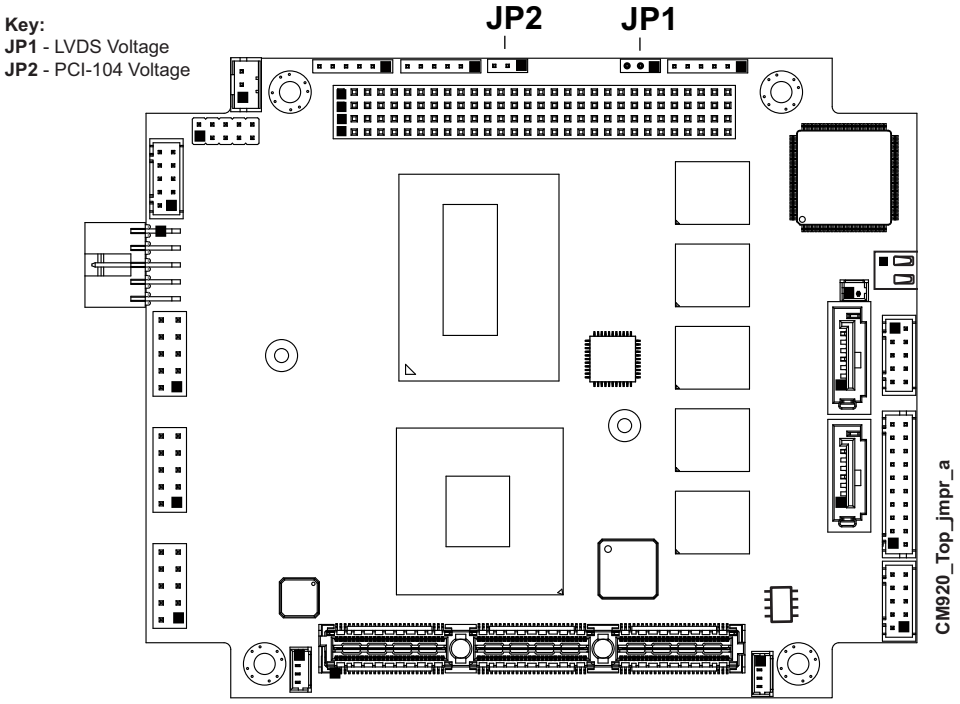

Figure 2-7. Jumper Header Locations (Top Side)

Specifications

Physical Specifications

Table 2-4 provides the physical dimensions of the CoreModule 920.

Table 2-4. Weight and Footprint Dimensions

Item	Dimension
Weight	0.12 kg (0.25 lbs)
Height (overall)	9.525mm (0.375 inches)
Board thickness	2.362mm (0.093 inches)
Width	96.01 mm (3.78 inches)
Length	102.87 mm (4.05 inches)

NOTE Overall height is measured from the upper board surface to the top of the highest permanent object (PCI-104 connector) on the upper board surface. This does not include the cooling solution, which is required on all versions of the board and may increase the height of the board. Component height should not exceed 0.345" (8.763mm) from the upper surface of the board and 0.190" (4.826mm) from the lower surface of the board. See Figure 2-10 on page 20 for the stack heights of the cooling solutions on the board.

Mechanical Specifications

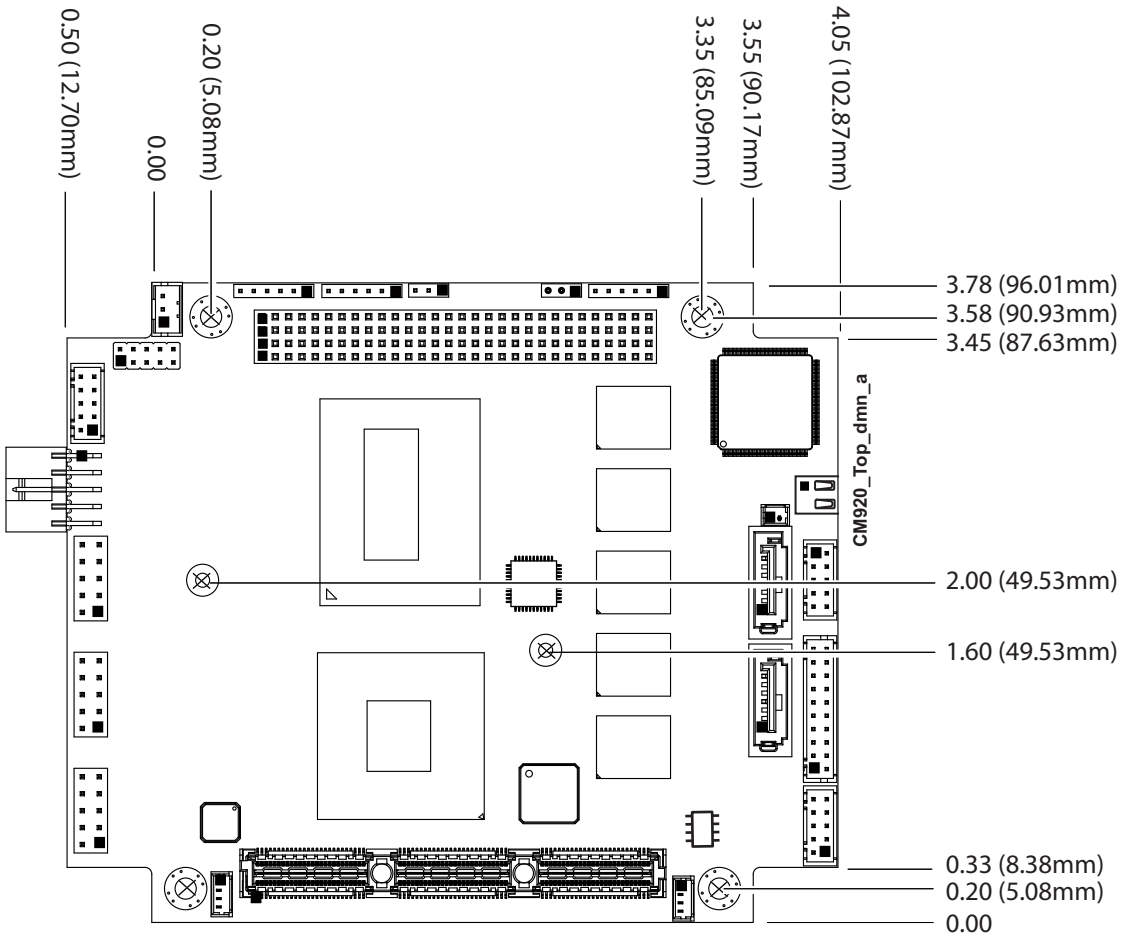

Figure 2-8. Mechanical Overview (Top Side)

NOTE	All dimensions are given in inches. Black square pins on headers and connectors represent pin 1. Black square pins on right-angle headers represent pin 2.

Power Specifications

Table 2-5 provides the current measurements for the CoreModule 920.

Table 2-5. Power Supply Requirements

Parameter	1.7GHz CPU (3517UE)
Input Type	Regulated DC voltages
In-Rush Peak Current and Duration	See Figure 2-9
Typical Idle Current and Power	1.68A (8.41W)
BIT Current and Power	4.41A (22.06W)

Operating configurations:

- In-rush operating configuration includes CRT monitor, 2GB memory, and power.
- Idle operating configuration includes In-rush configuration as well as one SATA 3.5" hard drive with Windows XP, one USB mouse, and one USB keyboard.
- BIT (Burn-In-Test) operating configuration includes Idle configuration as well as two USB thumb drives, two serial COM ports with loop backs, a second SATA hard drive as slave, and two Ethernet ports.

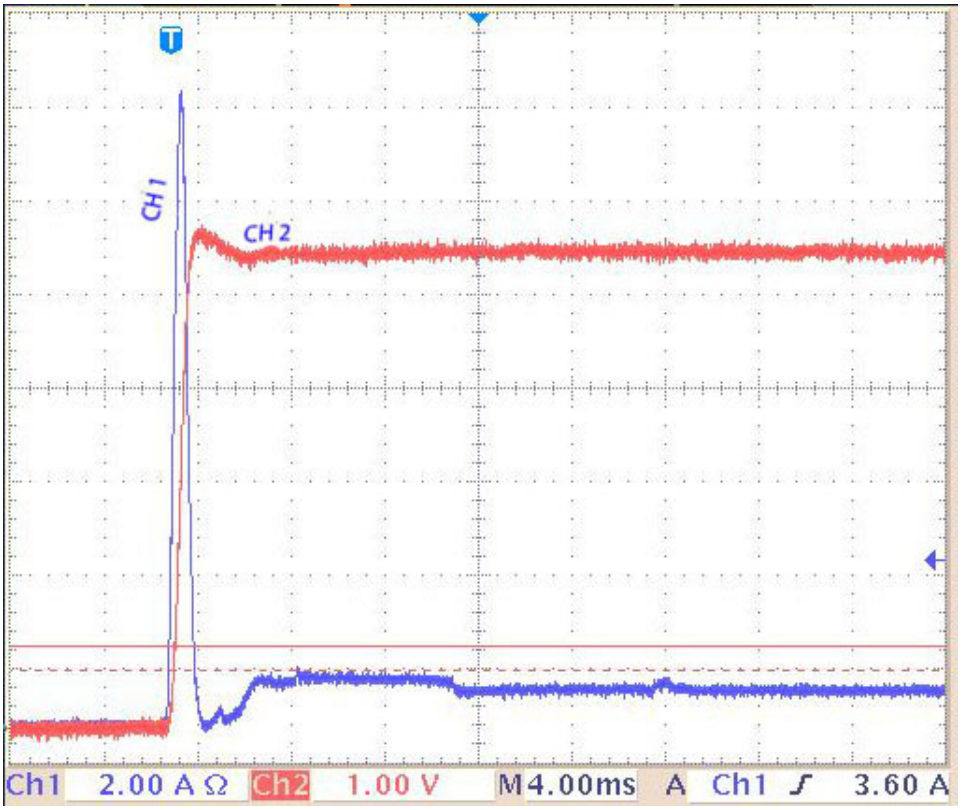

Figure 2-9. i7-3517UE Peak In-Rush Current and Duration

Environmental Specifications

Table 2-6 provides the most efficient operating and storage condition ranges required for this module.

Table 2-6. Environmental Requirements

Parameter	Conditions
Temperature	
Standard	–20° to +70° C (–4° to +158° F)
Extended (Optional)	–40° to +85° C (–40° to +185° F)
Storage	–55° to +85° C (–67° to +185° F)
Humidity	
Operating	5% to 90% relative humidity, non-condensing
Non-operating	5% to 95% relative humidity, non-condensing

Thermal/Cooling Requirements

The CPU is the primary source of heat on the board. The CoreModule 920 is designed to operate at the maximum speed of the CPU and requires an active heatsink for extended temperatures (optional). A passive heatsink is available (optional) and allows maximum speed operation within the Standard temperature range. The passive heatsink will allow operation in the Extended temperature range if the CPU speed is locked at 800MHz. To lock the CPU speed at 800MHz, use the Power Consumption setting field in the CPU/PPM Configuration submenu of the BIOS Setup Advanced menu. See Figure 2-10 for height measurements of the cooling assemblies.

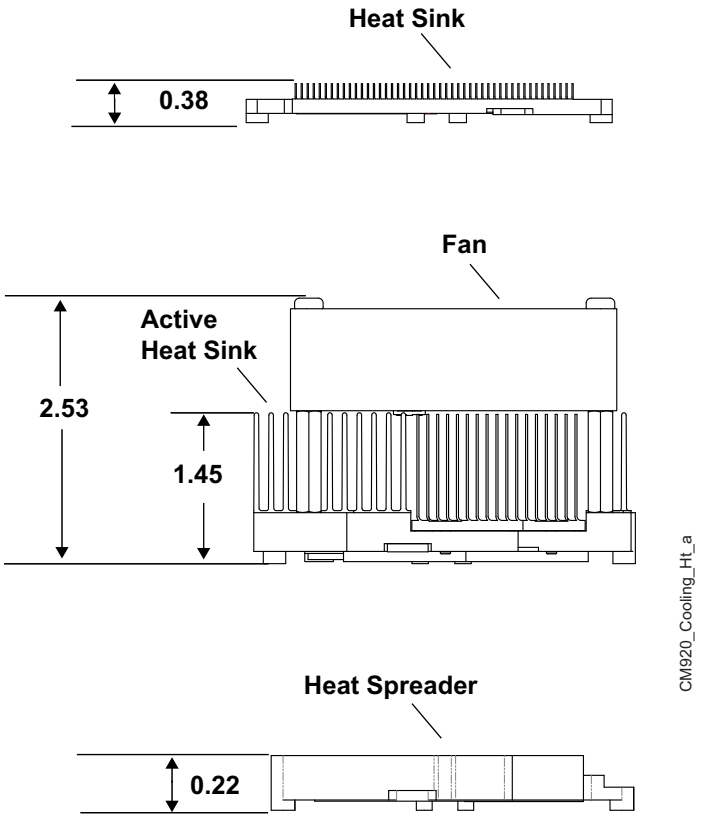

Figure 2-10. Stack Heights of Cooling Assemblies

NOTE All heights are given in inches.

Chapter 3 Hardware

Overview

This chapter discusses the chips and connectors of the module features in the following order:

- CPU
- Graphics
- Memory
- Interrupt Channel Assignments
- Memory Map
- I/O Address Map
- Serial Port Interfaces
- USB Interfaces
- Ethernet Interface
- Video Interfaces
  - VGA
  - LVDS
  - HDMI
  - PEG
- Power Interface
- GPIO Interface
- Utility Interface
  - Power Button
  - Reset Switch
  - Speaker
- System Fan Interface
- Battery Interface
- Ethernet LED Interface
- Miscellaneous
  - SSD (Solid State Drive)
  - Time of Day/RTC
  - Oops! Jumper (BIOS Recovery)
  - Serial Console
  - Hot Cable
  - Hardware Temperature and Voltage Monitor
  - Watchdog Timer

NOTE ADLINK Technology, Inc. only supports the features and options listed in this manual. The main components used on the CoreModule 920 may provide more features or options than are listed in this manual. Some of these features and options are not supported on the module and will not function as specified in the chip documentation.

The pin-out tables only of non-standard headers and connectors are included in this chapter. This chapter does not include pin-out tables for standard headers, connectors, and sockets such as SATA, PCI-104, and PCIe/104. Refer to references in Chapter 1 for PCI-104 and PCIe/104 pin outs.

CPU

The CoreModule 920 features one version of the Intel® Core™ i7 series CPU—the i7-3517UE—operating at 1.7GHz. The CPU integrates a high-performance 64-bit, x86 Processor Core with Memory Controller and 3D Graphics Engine. This single chip is based on 22-nm process technology and provides two execution cores, an Intel Flexible Display Interface, and a Direct Media Interface for high-speed connectivity to the PCH. The CPU also supports Intel Hyper-Threading Technology and up to 3.2GB of DDR3 SDRAM memory at 1333MHz for high overall performance.

Graphics

The CPU provides a refresh of the seventh generation graphics core, which features a substantial gain in performance and a decrease in power consumption. The next generation Intel Clear Video HD Technology includes a collection of video playback and enhancement features that improve the end user's viewing experience including Encode/Transcode HD content, HD content playback, and superior image quality. Other graphics features of the CPU include support for DirectX 11.0, OpenGL 3.1, DirectX Video Acceleration (DXAV), Advanced Scheduler 2.0, 1.0, and XPDM.

Memory

The CoreModule 920 employs one 1333MHz memory channel with one rank of eight system memory chips (and one additional chip for ECC). The board provides up to 2GB of extended memory using 2Gb DDR3 SDRAM chips. The CPU features Intel FMA (Fast Memory Access) technology, providing Just-in-Time Scheduling for issuing concurrent requests, Command Overlap for issuing multiple overlapping commands, and Out-of-Order Scheduling to re-order requests made to the same open page.

Interrupt Channel Assignments

The interrupt channel assignments are shown in Table 3-1.

Table 3-1. Interrupt Channel Assignments

Device vs IRQ No.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer	X															
Secondary Cascade			X													
COM1				O	D											
COM2				D	O											
RTC									X							
Math Coprocessor														X		
SATA Primary															X	
SATA Secondary																X
PCI INTA	Automatically Assigned															
PCI INTB	Automatically Assigned															
PCI INTC	Automatically Assigned															
PCI INTD	Automatically Assigned															
USB	Automatically Assigned															
Video	Automatically Assigned															
Ethernet	Automatically Assigned															

Legend: D = Default, O = Optional, X = Fixed

NOTE The IRQs for USB, Video, and Ethernet are automatically assigned by the BIOS Plug and Play logic. Local IRQs assigned during initialization can not be used by external devices.

Memory Map

The following table provides the common PC/AT memory allocations. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-2. Memory Map

Base Address			Function
00000000h	-	0009FFFFh	Conventional Memory
000A0000h	-	000AFFFFh	Graphics Memory
000B0000h	-	000B7FFFh	Mono Text Memory
000B8000h	-	000BFFFFh	Color Text Memory
000C0000h	-	000CFFFFh	Standard Video BIOS
000D0000h	-	000DFFFFh	DVMT Memory
000E0000h	-	000EFFFFh	PCI Express Base Memory
000F0000h	-	000FFFFFh	System Flash and PCI Resources

I/O Address Map

Table 3-3 shows the I/O address map. These are DOS-level addresses. The OS typically hides these physical addresses by way of memory management.

Table 3-3. I/O Address Map

Address (hex)	Subsystem
0000-00F	Primary DMA Controller
0020-0021	Master Interrupt Controller
0040-0043	Programmable Interrupt Timer (Clock/Timer)
0061	NMI, Speaker control
0063	NMI Controller
0065	NMI Controller
0067	NMI Controller
0070-007F	CMOS RAM, NMI Mask Reg, RT Clock
0080	System reserved
0081-0083	DMA Page Registers
0084-0086	System reserved
0087	DMA Page Register
0088	System reserved
0089-008B	DMA Page Registers
008C-008E	System reserved
008F	DMA Page Register
0090-0091	System reserved
0092	Fast A20 gate and CPU reset
0093-009F	System reserved
00A0-00A1	Slave Interrupt Controller
00A2-00BF	System reserved
00C0-00DF	Slave DMA Controller #2
00E0-00EF	System reserved
00F0-00FF	Math Coprocessor
01F0-01F7	SATA Controller
02F8-02FF	Serial Port 2 (COM2)
03B0-03BB	Video (monochrome)
03C0-03DF	Video (VGA)
03F8-03FF	Serial Port 1 (COM1)
0400-041F	SMBus Configuration Ports
0500-053F	PCH GPIO Configuration Ports
0800-087F	PCH Power Management Ports
0CF8-0CFF	PCI bus Configuration Address and Data

Serial Interfaces

The CoreModule 920 provides two RS-232 serial ports. The PCH BD82QM67 contains the circuitry for both serial ports and delivers the signals through two RS-232 transceivers: one transceiver for COM1 and the second transceiver for COM2. The serial ports support the following features:

- Two individual high-speed NS16C550A-compatible UARTs (COM1 and COM2)
- Programmable word length, stop bits, and parity
- 16-bit programmable baud rate generator
- Loop-back mode
- Two individual 16-bit FIFOs
- Serial Port Headers
  - J18 - Serial 1 (COM1) supports RS-232 and full modem
  - H16 - Serial 2 (COM2) supports RS-232 and full modem

Table 3-4 defines the pins and corresponding signals for serial 1 header (J18), which consists of 10 pins, 2 rows, odd/even sequence (1, 2), and 0.079" (2mm) pitch.

Table 3-4. Serial 1 (COM1) Interface Pin Signal Descriptions (J18)

Pin #	Signal	DB9 Pin #	Description
1	S1_DCD*	1	COM1 Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	S1_DSR*	6	COM1 Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	S1_RXD	2	COM1 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete.
4	S1_RTS*	7	COM1 Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
5	S1_TXD	3	COM1 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
6	S1_CTS*	8	COM1 Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	S1_DTR*	4	COM1 Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	S1_RI*	9	COM1 Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	GND	10	Ground

Note: The shaded table cell denotes ground. The * symbol indicates the signal is Active Low.

Table 3-4 defines the pins and corresponding signals for the Serial 2 header, which consists of 10 pins, 2 rows, odd/even sequence (1, 2), and 0.100" (2.54mm) pitch.

Table 3-5. Serial 2 (COM2) Interface Pin Signal Descriptions (H16)

Pin #	Signal	DB9 Pin #	Description
1	S2_DCD*	1	COM2 Data Carrier Detect – Indicates external serial device is detecting a carrier signal (i.e., a communication channel is currently open). In direct connect environments, this input is driven by DTR as part of the DTR/DSR handshake.
2	S2_DSR*	6	COM2 Data Set Ready – Indicates external serial device is powered, initialized, and ready. Used as hardware handshake with DTR for overall readiness.
3	S2_RXD	2	COM2 Receive Data – Serial port receive data input is typically held at a logic 1 (mark) when no data is being transmitted, and is held “Off” for a brief interval after an “On” to “Off” transition on the RTS line to allow the transmission to complete.
4	S2_RTS*	7	COM2 Request To Send – Indicates serial port is ready to transmit data. Used as hardware handshake with CTS for low level flow control.
5	S2_TXD	3	COM2 Transmit Data – Serial port transmit data output is typically held to a logic 1 when no data is being sent. Typically, a logic 0 (On) must be present on RTS, CTS, DSR, and DTR before data can be transmitted on this line.
6	S2_CTS*	8	COM2 Clear To Send – Indicates external serial device is ready to receive data. Used as hardware handshake with RTS for low level flow control.
7	S2_DTR*	4	COM2 Data Terminal Ready – Indicates serial port is powered, initialized, and ready. Used as hardware handshake with DSR for overall readiness.
8	S2_RI*	9	COM2 Ring Indicator – Indicates external serial device is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel.
9	GND	5	Ground
10	GND	10	Ground

Note: The shaded table cells denote ground. The * symbol indicates the signal is Active Low.

USB Interface

The CoreModule 920 contains two root USB hubs and six functional USB ports. Four of the six USB ports are routed through two 10-pin headers (H15 and J25), and the other two ports are routed through the PCIe/104 interface connector. The PCH provides the USB function including the following features:

- Supports USB v.2.0 EHCI and USB v.1.1 UHCI
- Provides over-current detection status
- Provides a fuse on board for over-current protection

Table 3-6 describes the pin signals of the USB0 and USB1 header which consists of 10 pins, in two rows, with odd/even (1, 2) pin sequence, and 0.100" (2.54mm) pitch.

Table 3-6. USB0 and USB1 Interface Pin Signals (H15)

Pin #	Signal	Description
1	USB-PWR_0	USB0 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
2	USB-PWR_1	USB1 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
3	CONN_USB0_N	USB0 Port Data Negative
4	CONN_USB1_N	USB1 Port Data Negative
5	CONN_USB0_P	USB0 Port Data Positive
6	CONN_USB1_P	USB1 Port Data Positive
7	USB_GND0	USB0 Ground
8	USB_GND1	USB1 Ground
9	USB_GND0	USB0 Ground
10	USB_GND1	USB1 Ground

Note: The shaded table cells denote power or ground.

Table 3-7 describes the pin signals of the USB2 and USB3 header, which consists of 10 pins in two rows, with odd/even (1, 2) pin sequence, and 0.079" (2mm) pitch.

Table 3-7. USB2 and USB3 Interface Pin Signals (J25)

Pin #	Signal	Description
1	USB-PWR_2	USB2 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
2	USB-PWR_3	USB3 Power – VCC (+5V +/-5%) power goes to the port through an on-board fuse. Port is disabled if this input is low.
3	CONN_USB2_N	USB2 Port Data Negative
4	CONN_USB3_N	USB3 Port Data Negative
5	CONN_USB2_P	USB2 Port Data Positive
6	CONN_USB3_P	USB3 Port Data Positive
7	USB_GND2	USB2 Ground
8	USB_GND3	USB3 Ground
9	USB_GND2	USB2 Ground
10	USB_GND3	USB3 Ground

Note: The shaded table cells denote power or ground.

Ethernet Interfaces

The CoreModule 920 supports two Gigabit Ethernet interfaces. The first Ethernet interface originates from the 82579LM PHY transceiver, which occupies one PCI Express lane and supports the internal MAC (Media Access Controller) in the PCH. The second Ethernet interface is implemented through the 82574IT Ethernet controller, which occupies one PCI Express lane and generates its own Gigabit Ethernet signals. The Ethernet function supports multi-speed operation at 10/100/1000 Mbps and operates in full-duplex at all supported speeds or half duplex at 10/100 Mbps while adhering to the IEEE 802.3x flow control specification. The Ethernet interface offers the following features:

- Full duplex support at 10 Mbps, 100 Mbps, or 1000 Mbps
- Half duplex support at 10 Mbps and 100 Mbps
- In full duplex mode, the Ethernet controller adheres to the IEEE 802.3x Flow Control specification
- In half duplex mode, performance is enhanced by a proprietary collision reduction mechanism
- IEEE 802.3 compatible physical layer to wire transformer
- IEEE 802.3u Auto-Negotiation support
- Fast back-to-back transmission support with minimum interframe spacing (IFS)
- IEEE 802.3x auto-negotiation support for speed and duplex operation
- On-board magnetics (Ethernet isolation transformers)

Table 3-8 describes the pin signals of the Ethernet GLAN1 interface, which consists of a two-row, 10-pin vertical header with odd/even (1,2) pin sequence, and 0.100" (2.54mm) pitch.

Table 3-8. GLAN1 Interface Pin Signal Descriptions (H11)

Pin #	Signal	Description
1	MDI1+	Media Dependent Interface 1 +/-
2	MDI1-	
3	MDI2+	Media Dependent Interface 2 +/-
4	MDI2-	
5	MDI0+	Media Dependent Interface 0 +/-
6	MDI0-	
7	MDI3+	Media Dependent Interface 3 +/-
8	MDI3-	
9	GND	Ground
10	GND	

Note: The shaded table cells denote ground.

NOTE The magnetics (isolation transformer, T1) for the Ethernet connector is included on the CoreModule 920.

Table 3-9 describes the pin signals of the Ethernet GLAN2 interface, which consists of a two-row, 10-pin vertical header with odd/even (1,2) pin sequence, and 0.079" (2mm) pitch.

Table 3-9. GLAN2 Interface Pin Signal Descriptions (J14)

Pin #	Signal	Description
1	MDI1+	Media Dependent Interface 1 +/-
2	MDI1-	
3	MDI2+	Media Dependent Interface 2 +/-
4	MDI2-	
5	MDI0+	Media Dependent Interface 0 +/-
6	MDI0-	
7	MDI3+	Media Dependent Interface 3 +/-
8	MDI3-	
9	GND	Ground
10	GND	

Note: The shaded table cells denote ground.

NOTE The magnetics (isolation transformer, T2) for the Ethernet header is included on the CoreModule 920.

Video Interfaces

The Core i7, 3517UE CPU provides an integrated 2D/3D graphics engine, which supports video decode such as MPEG2, VC-1, and AVC/H.264 (main, baseline at L3 and High-profile level 4.0/4.1) as well as video encode such as MPEG2, AVC/H.264 (baseline at L3), and VGA. The PCH supports VGA, LVDS, and HDMI display ports, permitting simultaneous, independent operation of two displays. The CPU provides PCIe x16 Graphics signals to the PCIe/104 connector for an external high-performance PCI Express Graphics card or other general purpose PCI Express devices. The video interface features are listed in the following bullets. Refer to Table 3-10 for definitions of the VGA pin signals and Table 3-11 for the LVDS pin signal definitions. The HDMI interface is a standard HDMI micro connector, and those pin signals are not defined in this manual. The PEG signals are part of the standard PCIe/104 interface and are not defined in this manual.

VGA:

- Supports resolutions up to 2048x1536 pixels at 75Hz
- Provides integrated 340.4MHz RAMDAC with 32-bit color
- Provides RGB output by three 8-bit DACs
- Supports HSYNC and VSYNC output

LVDS:

- Supports a maximum resolution of 1400x1050 at 60Hz (pixel clock rate up to 112MHz)
- Supports minimum pixel clock rate of 25MHz
- Supports a single channel interface through a 20-pin header
- Supports pixel color depths of 18 and 24 bits

HDMI:

- Supports resolutions up to 3840x2160 pixels at 30Hz
- Supports pixel clock rates from 25MHz to 340MHz

- Supports DVD-Audio and Audio Return channel
- Provides one 19-pin, standard HDMI micro connector

PEG (PCI Express Graphics):

- Supports external high-performance PCI Express graphics cards
- Supports general-purpose PCI Express devices
- Supports theoretical bandwidth of up to 8GT/s
- Provides PCIe Gen3 compliance

Table 3-10 defines the signals of the VGA interface, which consists of 10 pins, 2 rows, odd/even, (1, 2) with 0.079" (2mm) pitch.

Table 3-10. VGA Interface Pin Signal Descriptions (J17)

Pin #	Signal	Description
1	VSYNC	Vertical Sync – This signal is used for the digital vertical sync (polarity is programmable) 2.5V output to the VGA display.
2	HSYNC	Horizontal Sync – This signal is used for the digital horizontal sync (polarity is programmable) or “sync interval” 2.5V output to the VGA display
3	DDC-CLK	Display Control Clock
4	RED	Red – This is the Red analog output signal to the VGA display.
5	DDC-DATA	Display Control Data
6	GREEN	Green – This is the Green analog output signal to the VGA display.
7	VDD5V0	Power – This is the +5 volts +/- 5% power signal from the external power interface.
8	BLUE	Blue – This is the Blue analog output signal to the VGA display.
9	GND	Ground
10	GND	Ground

Note: The shaded table cells denote power or ground.

Table 3-11 lists the pin signals of the LVDS video header, which provides 20 pins, 2 rows, odd/even pin sequence (1, 2) with 0.079" (2mm) pitch.

Table 3-11. LVDS Video Interface Pin Signals (J23)

Pin #	Signal	Description
1	+12V	+12 volts for flat panel and backlight
2	VCC_LVDS_CONN	JP3 determines LVDS voltage (+3.3V or +5V)
3	GND	Ground
4	GND	Ground
5	LVDSA_CLK_P	LVDS A Clock Positive
6	LVDSA_CLK_N	LVDS A Clock Negative
7	LVDSA_DAT3_P	LVDS A DATA Positive Line 3
8	LVDSA_DAT3_N	LVDS A DATA Negative Line 3
9	LVDSA_DAT2_P	LVDS A DATA Positive Line 2
10	LVDSA_DAT2_N	LVDS A DATA Negative Line 2
11	LVDSA_DAT1_P	LVDS A DATA Positive Line 1
12	LVDSA_DAT1_N	LVDS A DATA Negative Line 1

Table 3-11. LVDS Video Interface Pin Signals (J23) (Continued)

Pin #	Signal	Description
13	LVDSA_DAT0_P	LVDS A DATA Positive Line 0
14	LVDSA_DAT0_N	LVDS A DATA Negative Line 0
15	LBKLT_CTL	Panel Backlight Control
16	LVDD_EN	Enable Panel Power
17	LDDC_CLK	Display Data Channel Clock
18	LDDC_DATA	Display Data Channel Data
19	LBKLT_EN	Enable Backlight Inverter
20	NC	Not Connected

Note: The shaded table cells denote power or ground.

Power Interface

The CoreModule 920 requires one +5 volt DC power source and provides a shrouded 10-pin, right-angle header with 2 rows, odd/even pin sequence (1, 2), and 0.100" (2.54mm) pitch.

The power input header (J24) supplies the following voltage and ground directly to the module:

- 4.75VDC - 5.0VDC +/- 5%

Table 3-12. Power Interface Pin Signals (J24)

Pin	Signal	Descriptions
1	GND	Ground
2	+5V	+5 Volts
3	GND	Ground
4	+12V	+12 Volts routed to PC/104, PC/104-Plus, and LVDS interfaces
5	GND	Ground
6	+3.3V_PCI	+3.3 Volts routed to PCI
7	GND	Ground
8	+5V	+5 Volts
9	GND	Ground
10	+5V	+5 Volts

Note: The shaded table cells denote power or ground.

User GPIO Interface

The CoreModule 920 provides GPIO pins for customer use, routing the signals from the PCH chipset to the J26 and J27 headers. An example test application and source code reside in each BSP directory of the CoreModule 920 Support Software QuickDrive.

For instructions on using the example applications, refer to the GPIO Readme in each BSP directory of the QuickDrive. For more information about the GPIO pin operation, refer to the PCH BD82QM67 datasheet at:

http://www.intel.com/Assets/PDF/datasheet/324645.pdf

Table 3-13 describes the pin signals of the GPIO1 interface, which provides a 6-pin, single-row header with 0.079" (2mm) pitch.

Table 3-13. User GPIO1 Interface Pin Signal Descriptions (J26)

Pin #	Signal	Description
1	PCH_GPIO71	User defined
2	PCH_GPIO70	User defined
3	PCH_GPIO69	User defined
4	PCH_GPIO68	User defined
5	GND	Ground
6	GND	Ground

Note: The shaded areas denote ground. All GPIO pins are in the Core Power Well of the PCH.

Table 3-14 describes the pin signals of the GPIO2 interface, which provides a 6-pin, single-row header with 0.079" (2mm) pitch.

Table 3-14. User GPIO2 Interface Pin Signal Descriptions (J27)

Pin #	Signal	Description
1	PCH_GPIO35	User defined
2	PCH_GPIO36	User defined
3	PCH_GPIO37	User defined
4	PCH_GPIO38	User defined
5	GND	Ground
6	GND	Ground

Note: The shaded table cells denote ground. All GPIO pins are in the Core Power Well of the PCH.

Utility Interface

The Utility interface provides three I/O signals on the module and consists of a 5-pin, 0.100" (2.54mm), single-row header (J21). The CPU drives the Power Button and Speaker signals on the Utility interface. A separate Power Management microprocessor drives the Reset Switch signal. Table 3-15 provides the signal definitions.

- Power Button
- Reset Switch
- Speaker

Power Button

The Utility header provides a signal for an external Power Button through pins 1 and 2. The Power Button allows the user to shut down and power on the system. To shut down the system, press and hold the Power Button for four seconds. Press the Power Button for one second to power on the system.

Reset Switch

Pins 2 and 3 on the Utility header provide the signals for an external reset button, which allows the user to re-boot the system.

Speaker

The speaker signal provides sufficient signal strength to drive an external 1W 8 Ω “Beep” speaker at an audible level through pins 4 and 5 on the Utility header. The speaker signal is driven from an on-board amplifier and the CPU.

Table 3-15 describes the pin signals of the Utility interface, which provides a 5-pin, single-row header with 0.100" (2.54mm) pitch.

Table 3-15. Utility Interface Pin Signals (J21)

Pin #	Signal	Description
1	PWR_BTN*	External Power Button (Pins 1-2)
2	GND	Ground
3	RESET SW*	External Reset Switch signal (Pins 2-3)
4	5V	+5 Volts Power
5	SPKR_CONN	Speaker Output (Pins 4-5)
6	GND	Ground

Note: The shaded table cells denote power or ground. The * symbol indicates the signal is Active Low.

System Fan

Table 3-16 lists the pin signals of the System Fan header, which provides a single row of 3 pins with 0.079" (2mm) pitch.

Table 3-16. System Fan Pin Signals (J22)

Pin #	Signal	Description
1	+V_FAN	+5.0 volts DC +/- 5%
2	NC	Not Connected
3	GND	Ground

Note: The shaded table cells denote power or ground.

Battery

Table 3-17 lists the pin signals of the External Battery Input header for backup CMOS RAM and RTC (Real Time Clock), which uses 2 pins with 0.049" (1.25mm) pitch.

Table 3-17. External Battery Input Header (J12)

Pin #	Signal	Description
1	3.3_BATT	+3.3 volts DC +/- 5%
2	GND	Ground

Note: The shaded table cells denote power or ground. The RTC has an expected current draw of 6µA at room temperature, with +3.3V.

External LEDs (Ethernet)

These two headers provide signals for two external LEDs that indicate Ethernet links and activity.

Table 3-18 defines the signals for the GLAN1 LED header that indicates Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-18. GLAN1 External LED Pin Signals (J2)

Pin #	Signal	Description
1	V3.3_CONN	+3.3 volts – Provides +3.3 volts to external LED (Pins 1-2 for Green LED)
2	GBE1_ACT_LED	Ethernet Activity
3	GBE1_LINK1000_LED	Gigabit Ethernet Link
4	GBE1_LINK100_LED	Fast Ethernet Link with +3.3 volts power (Pins 3-4 for Bi-Color LED)

Note: The shaded table cell denotes power. Configure Ethernet LEDs for Active Low operation.

Table 3-19 defines the signals for the GLAN2 LED header that indicates Ethernet links and activity using a single row of 4 pins with 0.049" (1.25mm) pitch.

Table 3-19. GLAN2 External LED Pin Signals (J3)

Pin #	Signal	Description
1	V3.3_CONN	+3.3 volts – Provides +3.3 volts to external LED (Pins 1-2 for Green LED)
2	GBE2_ACT_LED	Ethernet Activity
3	GBE2_LINK1000_LED	Gigabit Ethernet Link
4	GBE2_LINK100_LED	Fast Ethernet Link with +3.3 volts power (Pins 3-4 for Bi-Color LED)

Note: The shaded table cell denotes power.

Miscellaneous

SSD (Solid State Drive)

The CoreModule 920 provides an 8GB SSD, which is soldered directly onto the board. For more information refer to the SSD data sheet: http://www.greenliant.com/products/solid_state_storage.dot#sn.

Real Time Clock (RTC)

The CoreModule 920 contains a Real Time Clock (RTC). The RTC can be backed up with a battery. If the battery is not present, the board BIOS has a battery-less boot option to complete the boot process.

Oops! Jumper (BIOS Recovery)

The Oops! jumper function is provided in the event the BIOS settings you have selected prevent you from booting the system. By using the Oops! jumper you can prevent the current BIOS settings in flash from being loaded, allowing you to boot using default settings.

Use a jumper to connect the DTR pin (4) to the RI pin (9) on Serial Port 1 (COM1) prior to boot up to prevent the present BIOS settings from loading. After booting with the Oops! jumper in place, remove the Oops! jumper and return to BIOS Setup. You must now load factory defaults by selecting *Restore Defaults* from the *Save & Exit* menu. Then select *Save Changes and Exit* to reboot the system. Now you can modify the default settings to your desired values. Ensure you save the changes before rebooting the system.

To convert a standard DB9 connector to an Oops! jumper, short together the DTR (4) and RI (9) pins on the front of the connector as shown in Figure 3-1 on the Serial Port 1 DB9 connector.

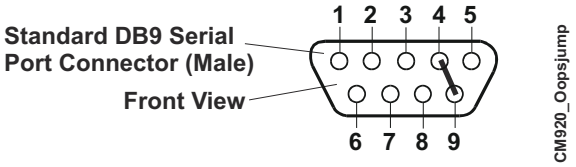

Figure 3-1. Oops! Jumper Serial Port (DB9)

Serial Console

The CoreModule 920 BIOS supports the serial console (or console redirection) feature. This I/O function is ANSI-compatible with a serial terminal or with equivalent terminal emulation software running on another system. This can be very useful when setting up the BIOS on a production line for systems that are not connected to a keyboard and display.

Serial Console Setup

The serial console feature is implemented by entering the serial console settings in the BIOS Setup Utility and connecting the appropriate serial cable (a standard null modem serial cable or "Hot Cable") between one of the serial ports (COM1) and the serial terminal or a PC with communications software. Refer to Chapter 4, BIOS Setup for the connection procedure, the serial console option settings, and the settings for the serial terminal, or PC with communications software.

Hot (Serial) Cable

To convert a standard serial cable to a "Hot Cable", short together the RTS (7) and RI (9) pins on the serial port cable DB9 connector as shown in Figure 3-2.

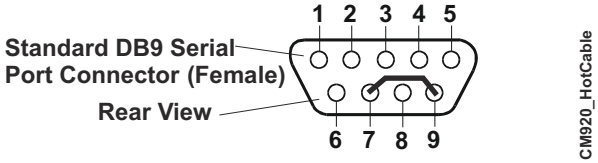

Figure 3-2. Serial Console Jumper

Hardware Voltage and Temperature Monitor

The CoreModule 920 provides a hardware monitor to ensure the health of your embedded system with built-in support for monitoring and control of system temperatures, fan speeds, and critical module voltage levels. The ADT 7490 Hardware Monitor BIOS setting resides in the Advanced menu of the BIOS setup utility. See Chapter 4, “BIOS Setup” .

Watchdog Timer

The Watchdog Timer (WDT) restarts the system if a mishap occurs, ensuring proper start up after the interruption. Possible problems include failure to boot properly, the application software’s loss of control, failure of an interface device, unexpected conditions on the bus, or other hardware or software malfunctions.

The WDT (Watchdog Timer) can be used both during the boot process and during normal system operation.

- During the Boot process – If the operating system fails to boot in the time interval set in the BIOS, the system will reset.

  Enable the WDT using *Watchdog Timer* of the Boot menu in BIOS Setup. Set the WDT for a time-out interval in seconds, between 1 and 255, in one-second increments in the Boot Configuration screen. Ensure you allow enough time for the boot process to complete and for the OS to boot. The OS or application must tickle the WDT as soon as it comes up. This can be done by accessing the hardware directly or through a BIOS call.

- During System Operation – An application can set up the WDT hardware through a BIOS call, or by accessing the hardware directly. Some ADLINK Board Support Packages provide an API interface to the WDT. The application must tickle the WDT in the time set when the WDT is initialized or the system will be reset. You can use a BIOS call to tickle the WDT or access the hardware directly.

- Watchdog Code examples – ADLINK has provided source code examples on the CoreModule 920 Support Software QuickDrive illustrating how to control the WDT. The code examples can be easily copied to your development environment to compile and test the examples, or make any desired changes before compiling. Refer to the WDT Readme file on the CoreModule 920 Support Software QuickDrive.

Chapter 4 BIOS Setup

Introduction

This section assumes the user is familiar with general BIOS Setup and does not attempt to describe the BIOS functions. Refer to "BIOS Setup Menus " on page 39 in this chapter for a map of the BIOS Setup settings. If ADLINK has added to or modified any of the standard BIOS functions, these functions will be described.

Entering BIOS Setup (Local Video Display)

To enter BIOS Setup using a local video display for the CoreModule 920:

1. Turn on the display and the power supply to the CoreModule 920.
2. Start Setup by pressing the [Del] or [F2] keys (F2 allows you to load previous settings) when the following message appears on the boot screen.

```
Please wait. This will take a few seconds.
```

> **NOTE** If the setting for *Fast Boot* is [Enabled], the system may not enter the BIOS Setup if you do not press the <Del> or <F2> keys early in the boot sequence.

3. Follow the instructions on the right side of the screen to navigate through the selections and modify any settings.

Entering BIOS Setup (Serial Port Console)

This section describes how to enter the BIOS setup through a remote serial terminal or PC.

1. Turn on the power supply to the CoreModule 920 and enter the BIOS Setup Utility using a local video display.
2. Ensure the BIOS feature *Serial Port Console Redirection* is set to [Enabled] under the **Advanced** menu.
3. Accept the default options or make your own selections for the balance of the Console Redirection fields and record your settings.
4. Ensure you select the type of remote serial terminal you will be using and record your selection.
5. Select *Save Changes and Exit* and then shut down the CoreModule 920.
6. Connect the remote serial terminal (or the PC with communications software) to the COM1 serial port on the CoreModule 920.
7. Turn on the remote serial terminal or PC and set it to the settings you selected earlier in the procedure.

   The default settings for the CoreModule 920 are:

   - ANSI
   - 115200
   - 8 bits
   - no parity
   - 1 stop bit
   - no flow control (None)
   - Disabled Recorder Mode
   - Disabled Resolution 100x31
   - [80x24] for Legacy OS Redirection

8. Restore power to the CoreModule 920.
9. Press the F2 key to enter Setup (early in the boot sequence if *Fast Boot* is set to [Enabled].)

   If *Fast Boot* is set to [Enabled], you may never see the screen prompt.
10. Use the <Enter> key to select the screen menus listed in the Opening BIOS screen.

> **NOTE** The serial console port is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

OEM Logo Utility

The CoreModule 920 BIOS supports a graphical logo utility, which allows the user to customize the boot screen image. The graphical image can be a company logo or any custom image the user wants to display during the boot process. The custom image can be displayed as the first image on screen during the boot process and remain there while the OS boots, depending on the options selected in BIOS Setup.

> **NOTE** The Quiet Boot feature must be set to Enabled in the Boot screen of BIOS Setup for the system to recognize the OEM Logo feature.

Logo Image Requirements

Please contact your ADLINK Sales Representative for more information on OEM Logo Utility requirements.

BIOS Setup Menus

This section provides illustrations of the six main setup screens in the CoreModule 920 BIOS Setup Utility. Below each illustration is a bullet list of the screen's submenus and setting selections. The setting selections are presented in brackets after each submenu or menu item, and the optimal default settings are presented in bold. For more detailed definitions of the BIOS settings, refer to the AMI Aptio TSE User Manual: http://www.ami.com/support/doc/AMI_TSE_User_Manual_PUB.pdf.

Table 4-1. BIOS Setup Menus

BIOS Setup Utility Menu	Item/Topic
Main	Language, Date, and Time
Advanced	ACPI, CPU, SATA, GPIO, USB, Hardware Monitor, Serial Ports, Serial Port Console
Chipset	PCH I/O, System Agent
Boot	Boot up Settings, Boot Options, Boot Order
Security	Setting or changing Passwords
Save & Exit	Exiting with or without changing settings, loading and restoring Optimal or User Defaults

Main BIOS Setup Screen

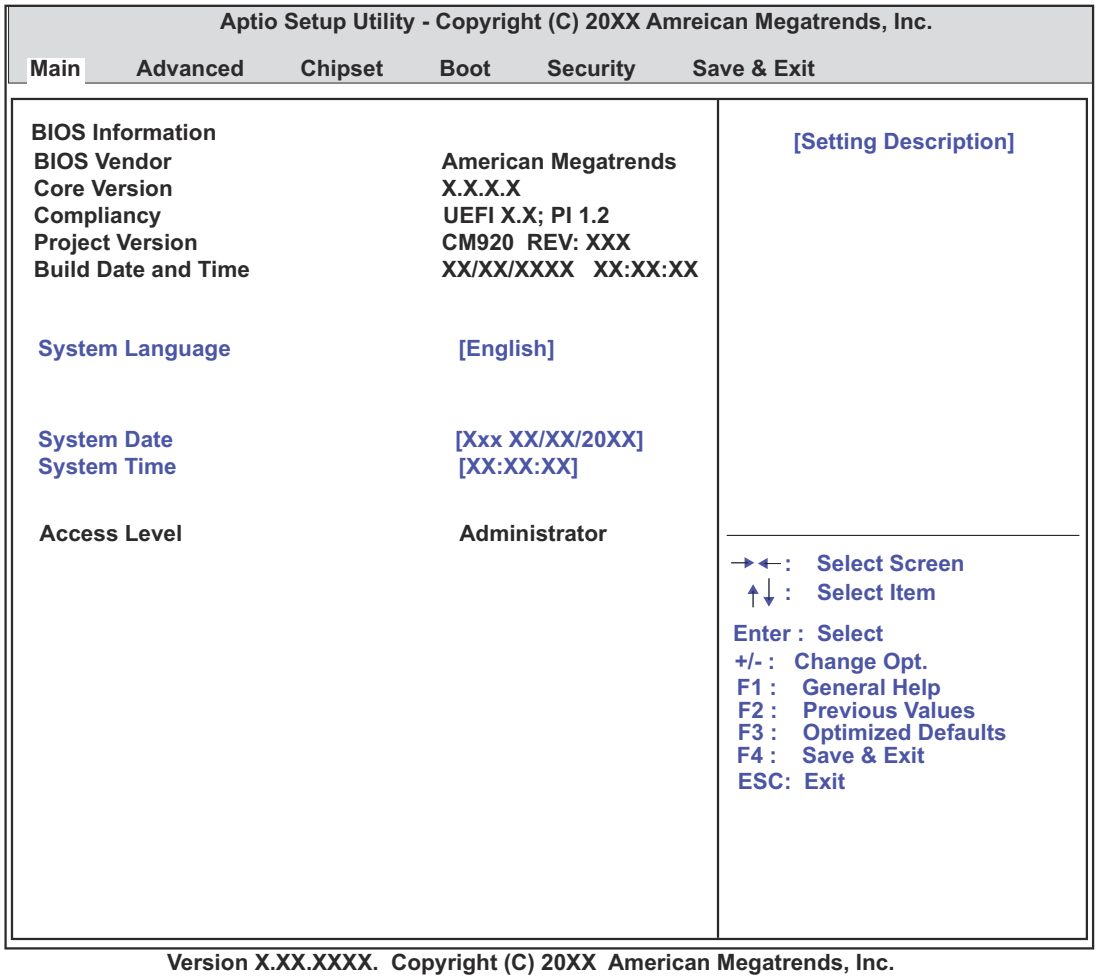

Figure 4-1. Main BIOS Setup Screen

- **System Language** **[English]**
- **System Date**

  System Date (day of week, mm:dd:yyyy) – This field requires the alpha-numeric entry of the day of week, day of the month, calendar month, and all 4 digits of the year, indicating the century plus year (*Fri XX/XX/20XX*).

- **System Time**

  System Time (hh:mm:ss) – This is a 24-hour clock setting in hours, minutes, and seconds.

Advanced BIOS Setup Screen

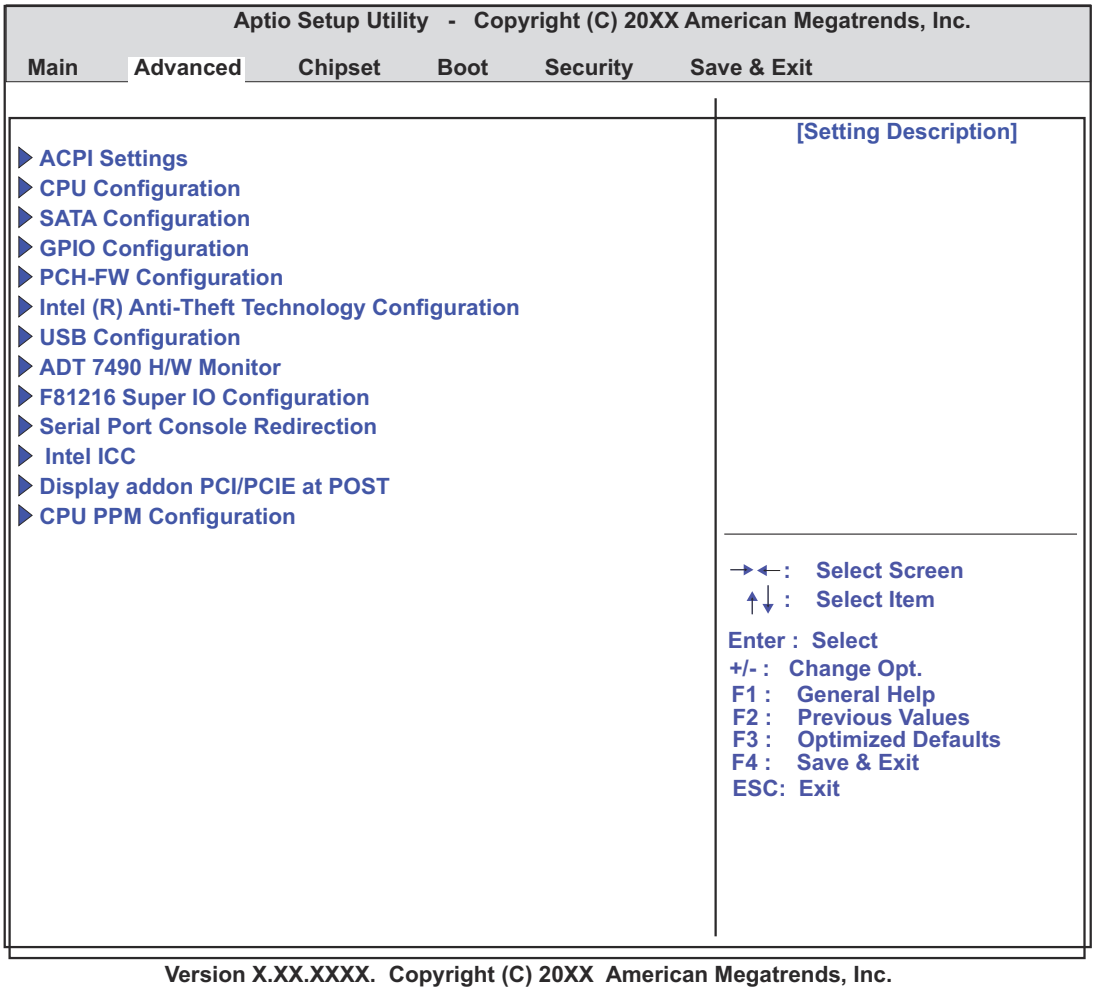

Figure 4-2. Advanced BIOS Setup Screen

- **ACPI Settings**
  - Enable Hibernation [Disabled; **Enabled**]
  - ACPI Sleep State [**S1 - CPU Stop Clock**]
- **CPU Configuration**
  - Intel(R) Core(TM) i7-3517UE @ 1.70GHz
  - CPU Signature XXXxX
  - Microcode Patch XX
  - Max CPU Speed XXXX MHz

- Min CPU Speed XXX MHz
- Processor Cores X
- Intel HT Technology Supported
- Intel VT-x Technology Supported
- Intel SMX Technology Supported
- 64-bit Supported

- L1 Data Cache 32 kB x 2
- L1 Code Cache 32 kB x 2
- L2 Cache 256 kB x 2
- L3 Cache 4096 kB x2

- Hyper-Threading [Disabled; **Enabled**]
- Active Processor Cores [**All**; 1]
- Limit CPUID Maximum [**Disabled**; Enabled]
- Execute Disable Bit [Disabled; **Enabled**]
- Intel Virtualization Technology [**Disabled**; Enabled]

- **SATA Configuration**
  - SATA Controller(s) [**Enabled**; Disabled]
  - SATA Mode Selection [**IDE**; AHCI; RAID]

  - Serial ATA Port 0 Empty
    - Software Preserve Unknown
  - Serial ATA Port 1 Empty
    - Software Preserve Unknown
  - Serial ATA Port 2 GLS85LS1008P C (X.XGB)
    - Software Preserve Supported
- **GPIO Configuration**
  - GPIO0 Mode [**Input**; Output]
  - GPIO1 Mode [**Input**; Output]
  - GPIO2 Mode [**Input**; Output]
  - GPIO3 Mode [**Input**; Output]
  - GPIO4 Mode [**Input**; Output]
  - GPIO5 Mode [**Input**; Output]
  - GPIO6 Mode [**Input**; Output]
  - GPIO7 Mode [**Input**; Output]

- **PCH-FW Configuration**
  - ME FW Version X.X.XX.XXXX
  - ME Firmware Mode Normal Mode
  - ME Firmware Type Full Sku Firmware
  - ME Firmware SKU XMB
- **Intel(R)Anti-Theft Technology Configuration**
  - Intel(R) Anti-Theft Technology [**Disabled**; Enabled]
  - Intel(R) Anti-Theft Technology Rec [**X**]
  - Enter Intel(R) AT Suspend Mode [**Disabled**]
- **USB Configuration**
  - USB Devices:
    X Keyboard, 2 Hubs
  - Legacy USB Support [**Enabled**; Disabled; Auto]
  - EHCI Hand-off [**Disabled**; Enabled]
  - USB hardware delays and time-outs:
    - USB transfer time-out [1 sec; 5 sec; 10 sec; **20 sec**]
    - Device reset time-out [10 sec; **20 sec**; 30 sec; 40 sec]
    - Device power-up delay [**Auto**; Manual]
- **ADT 7490 H/W Monitor**
  - ADT 7490 Pc Health Status
    - Module temperature : +XX C
    - ADT7490 temperature : +XX C
    - CPU temperature (By PECI) : +XX C
    - Vtt : +X.XXX V
    - Vccp : +X.XXX V
    - Vcc : +X.XXX V
    - +5V : +X.XXX V
    - +12V : +XX.XXX V
- **F81216 Super IO Configuration**
  - Super IO Chip Fintek F81216
  - F81216 Serial Port 1 Configuration
    - Serial Port [Disabled; **Enabled**]
    - Device Settings IO=3F8h; IRQ=4;
    - Change Settings [**Auto**;
      IO=3E8h; IRQ=7;
      IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
      IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
      IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
      IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
      IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
      IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12]

- F81216 Serial Port 2 Configuration
  - Serial Port [Disabled; **Enabled**]
  - Device Settings IO=2F8h; IRQ=3;
  - Change Settings [**Auto**;
    IO=2E8h; IRQ=10;
    IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
    IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
    IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
    IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
    IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
    IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12]
- F81216 Watchdog
  - Enable Watchdog [**Disabled**; Enabled]

- **Serial Port Console Redirection**
  - COM1
    - Console Redirection [**Disabled**; Enabled]
    - Console Redirection Settings
      - Terminal Type [VT100; VT100+; VT-UTF8; **ANSI**]
      - Bits per second [9600; 19200; 38400; 57600; **115200**]
      - Data Bits [7; **8**]
      - Parity [**None**; Even; Odd; Mark; Space]
      - Stop Bits [**1**; 2]
      - Flow Control [**None**; Hardware RTS/CTS]
      - VT-UTF8 Combo Key Support [Disabled; **Enabled**]
      - Recorder Mode [**Disabled**; Enabled]
      - Resolution 100x31 [**Disabled**; Enabled]
      - Legacy OS Redirection [**80x24**; 80x25]
      - Putty KeyPad [**VT100**; LINUX; XTERMR6; SCO; ESCN; VT400]
  - COM2
    - Console Redirection [**Disabled**; Enabled]
    - Console Redirection Settings
      - Terminal Type [VT100; VT100+; VT-UTF8; **ANSI**]
      - Bits per second [9600; 19200; 38400; 57600; **115200**]
      - Data Bits [7; **8**]
      - Parity [**None**; Even; Odd; Mark; Space]
      - Stop Bits [**1**; 2]
      - Flow Control [**None**; Hardware RTS/CTS]
      - VT-UTF8 Combo Key Support [Disabled; **Enabled**]
      - Recorder Mode [**Disabled**; Enabled]
      - Resolution 100x31 [**Disabled**; Enabled]
      - Legacy OS Redirection [**80x24**; 80x25]
      - Putty KeyPad [**VT100**; LINUX; XTERMR6; SCO; ESCN; VT400]

- COM (SOL) (Pci Bus0, Dev22, Func3)
  - Console Redirection [**Disabled**; Enabled]
  - Console Redirection Settings
    - Terminal Type [VT100; VT100+; VT-UTF8; **ANSI**]
    - Bits per second [9600; 19200; 38400; 57600; **115200**]
    - Data Bits [7; **8**]
    - Parity [**None**; Even; Odd; Mark; Space]
    - Stop Bits [**1**; 2]
    - Flow Control [**None**; Hardware RTS/CTS]
    - VT-UTF8 Combo Key Support [Disabled; **Enabled**]
    - Recorder Mode [**Disabled**; Enabled]
    - Resolution 100x31 [**Disabled**; Enabled]
    - Legacy OS Redirection [**80x24**; 80x25]
    - Putty KeyPad [**VT100**; LINUX; XTERMR6; SCO; ESCN; VT400]

NOTE The serial port console is not hardware protected. Diagnostic software that probes hardware addresses may cause a loss or failure of the serial console functions.

- **Intel ICC** (Integrated Clock Control options)
  - Use Watchdog timer for ICC [**Disabled**; Enabled]
  - Turn off unused PCI/PCIe clocks [**Disabled**; Enabled]
  - Lock ICC registers [**Static only**; All registers]
  - Clock Manipulation
  - ICC Overclocking Lib X.X.X.XX
  - DIV-1S
    - DIV-1S
    - GFX
    - Maximum supported frequency XXX.XX MHz
    - Minimum supported frequency XXX.XX MHz
    - Current frequency XXX.XX MHz
    - Current SSC mode Down
    - Current SSC % X.XX%

- DIV-2S
  - DIV-2S
  - Not used
  - Maximum supported frequency XXX.XX MHz
  - Minimum supported frequency XXX.XX MHz
  - Current frequency XXX.XX MHz
  - Current SSC mode Down
  - Current SSC % X.XX%
- DIV3
  - DIV3
  - Not used
  - Maximum supported frequency XXX.XX MHz
  - Minimum supported frequency XXX.XX MHz
  - Current frequency XXX.XX MHz
  - Current SSC mode Down
  - Current SSC % X.XX%
- DIV4
  - DIV4
  - GFX Bending
  - Maximum supported frequency XXX.XX MHz
  - Minimum supported frequency XXX.XX MHz
  - Current frequency XXX.XX MHz
  - Current SSC mode Down
  - Current SSC % X.XX%
- DIV-1NS
  - DIV-1NS
  - GFX
  - Maximum supported frequency XXX.XX MHz
  - Minimum supported frequency XXX.XX MHz
  - Current frequency XXX.XX MHz
  - Current SSC mode Down
  - Current SSC % X.XX%
- DIV-2NS
  - DIV-2NS
  - Not used
  - Maximum supported frequency XXX.XX MHz
  - Minimum supported frequency XXX.XX MHz
  - Current frequency XXX.XX MHz
  - Current SSC mode Down
  - Current SSC % X.XX%

- **Display addon PCI/PCIE at POST**
  - DAPP Enabled [**Disabled**; Enabled]
- **CPU PPM Configuration**
  - EIST (Intel SpeedStep) [Disabled; **Enabled**]
  - Turbo Mode [Disabled; **Enabled**]
  - Power Consumption [XXX]
  - CPU C3 Report [Disabled; **Enabled**]
  - CPU C6 Report [Disabled; **Enabled**]
  - CPU C7 Report [Disabled; **Enabled**]

Chipset BIOS Setup Screen

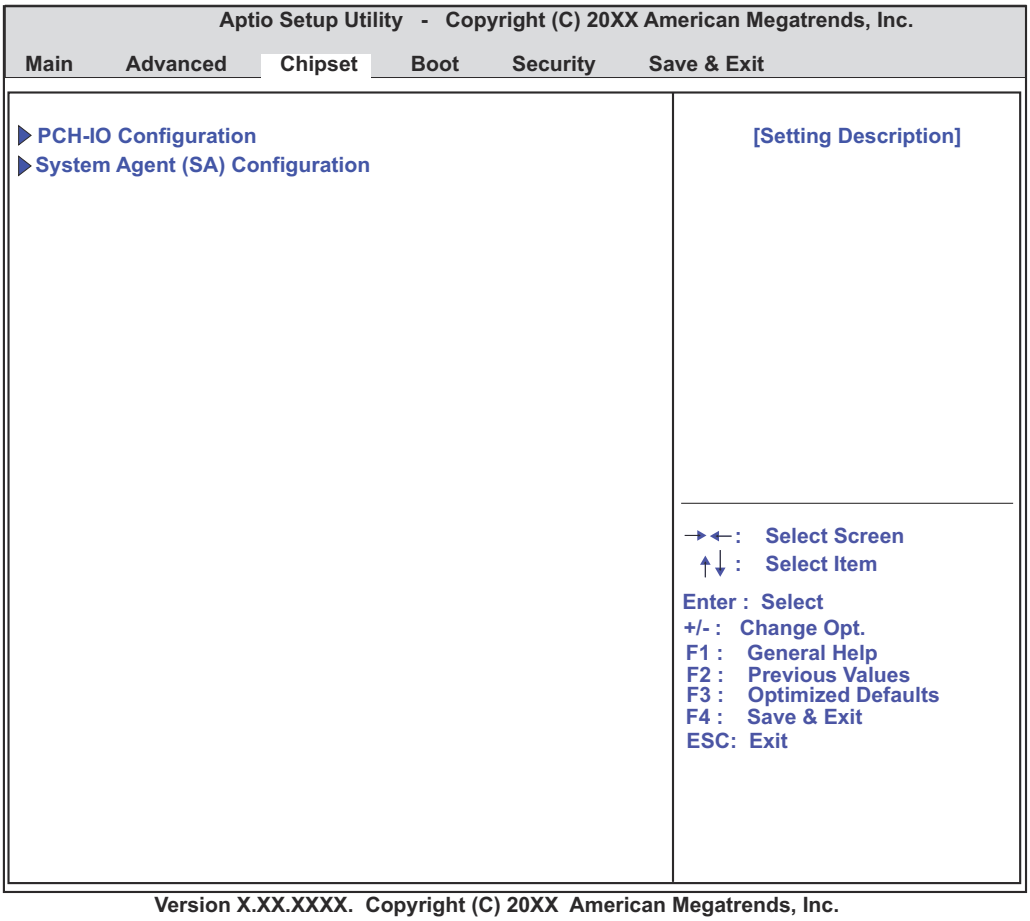

Figure 4-3. Chipset BIOS Setup Screen

- **PCH-IO Configuration**
  - Intel PCH RC Version X.X.X.X
  - Intel PCH SKU Name QM67
  - Intel PCH Rev ID XX/XX

- PCI Express Configuration
  - Subtractive Decode [Disabled; **Enabled**]
  - PCI Express Root Port 1 [Disabled; **Enabled**]
  - PCI Express Root Port 2 [Disabled; **Enabled**]
  - PCI Express Root Port 3 [Disabled; **Enabled**]
  - PCI Express Root Port 4 [Disabled; **Enabled**]
- USB Configuration
  - EHCI1 [Disabled; **Enabled**]
  - EHCI2 [Disabled; **Enabled**]
- PCH Azalia Configuration
  - Azalia [Disabled; Enabled; **Auto**]
- PCH LAN Controller [**Enabled**; Disabled]

- **System Agent (SA) Configuration**
  - System Agent Bridge Name IvyBridge
  - System Agent RC Version X.X.X.X
  - VT-d Capability Supported
  - VT-d [Disabled; **Enabled**]
  - Graphics Configuration
    - IGFX VBIOS Version XXXX
    - IGfx Frequency XXX MHz
    - Primary Display [**Auto**; IGFX; PEG]
    - Internal Graphics [Disabled; **Enabled**]
    - GTT Size [1MB; **2MB**]
    - Aperture Size [128MB; **256MB**; 512MB]
    - DVMT Pre-Allocated [32MB; **64M**; 96M; 128M; 160M; 192M; 224M; 256M; 288M; 320M; 352M; 384M; 416M; 448M; 480M; 512M; 1024M]
    - DVMT Total Gfx Mem [128MB; **256M**; MAX]
    - LCD Control

      - Primary IGFX Boot Display [Auto; **CRT**; CRT+LVDS; LVDS]

      - Video Function [HDMI]

      - LCD Panel Type [640x480 LVDS;

        800x600 LVDS;

        1024x768 LVDS;

        1280x1024 LVDS;

        1400x1050 (DCLK 108MHz);

        1400x1050 (DCLK 122MHz);

        1600x1200 LVDS;

        1366x768 LVDS;

1680x1050 LVDS;
1920x1200 LVDS;
1024x600 LVDS;
1280x600 LVDS;
1280x768 LVDS;
1280x800 LVDS;
1920x1080 LVDS;
2048x1536 LVDS]

- Active LFP [No LVDS; **Int-LVDS**]
- Panel Color Depth [18 Bit; **24 Bit**]
- GTT LVDS Backlight Control [0%; 20%; 40%; 60%; 80%; **100%**]
- GTT LVDS Backlight Inverter [PWM Inverted; **PWM Normal**]

♦ NB PCIe Configuration

- PEG0 XXXX
  - PEG0 - Gen X [**Auto**; Gen1; Gen2; Gen3]
  - PEG0 ASPM [Disabled; **Auto**; ASPM L0s; ASPM L1; ASPM L0sL1]

- Enable PEG [Disabled; Enabled; **Auto**]

♦ Memory Configuration

- Memory RC Version X.X.X.X
- Memory Frequency XXXX MHz
- Total Memory XXXX MB (DDR3)
- DIMM#0 XXXX MB (DDR3)
- DIMM#1 Not Present
- DIMM#2 Not Present
- DIMM#3 Not Present
- CAS Latency (tCL) X
- Minimum delay time
  - CAS to RAS (tRCDmin) X
  - Row Precharge (tRPmin) X
  - Active to Precharge (tRASmin) XX

Boot BIOS Setup Screen

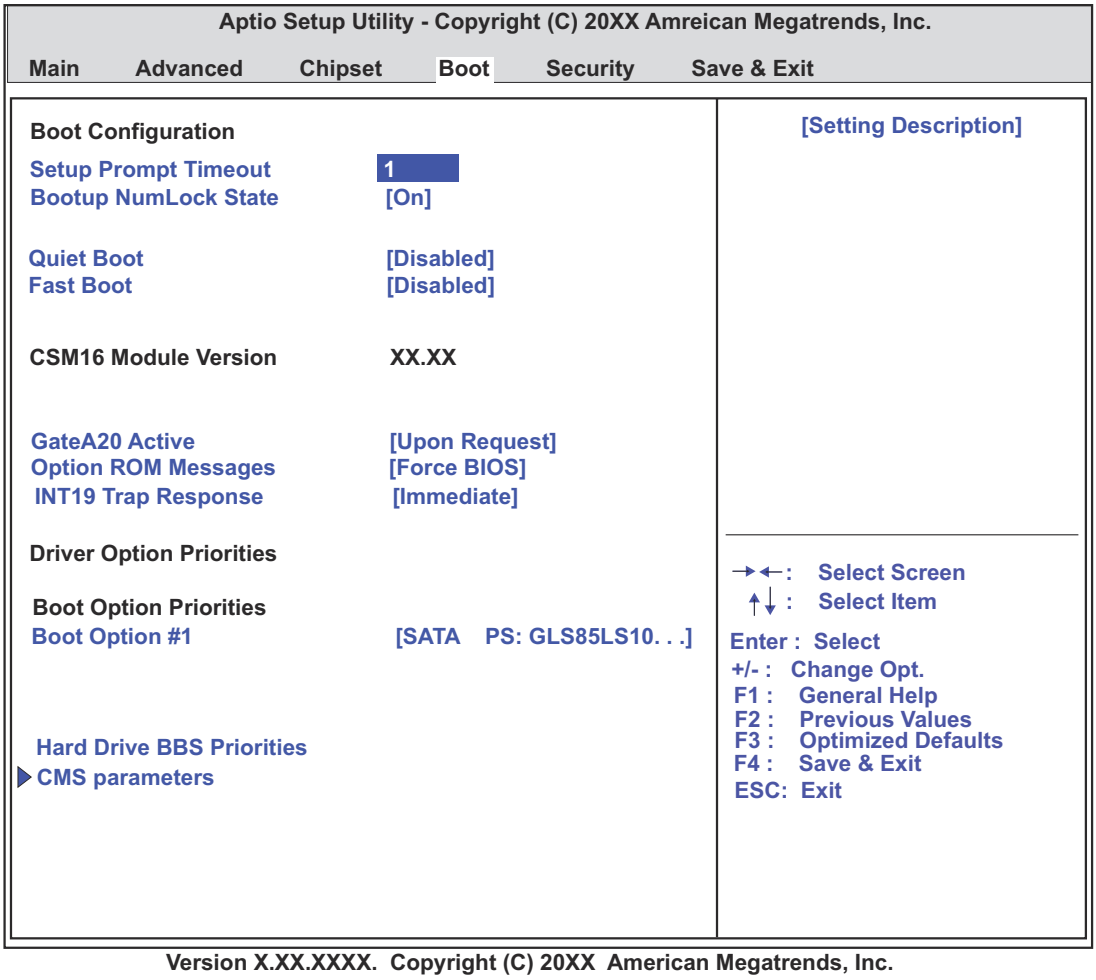

Figure 4-4. Boot BIOS Setup Screen

- **Boot Configuration**
  - Setup Prompt Timeout [**1**]
  - Bootup NumLock State [**On**; Off]
  - Quiet Boot [**Disabled**; Enabled]
  - Fast Boot [**Disabled**; Enabled]
- **CSM16 Module Version XX.XX**
  - Gate A20 Active [**Upon Request**; Always]
  - Option ROM Messages [**Force BIOS**; Keep Current]
  - INT19 Trap Response [**Immediate**; Postponed]
- **Driver Option Priorities**
- **Boot Option Priorities**
  - Boot Option #1 [**SATA PS: GLS85LS1008P CS XXGB**; Disabled]
  - Hard Drive BBS Priorities
    - Boot Option #1 [**P1-GLS85LS1032A CS 32GBN A101C0**; Disabled]

- CSM parameters
  - Launch CSM [**Always**; Never]
  - Boot option filter [**UEFI and Legacy**; Legacy only; UEFI only]
  - Launch PXE OpROM policy [**Do not launch**; UEFI only; Legacy only]
  - Launch Storage OpROM policy [Do not launch; UEFI only; **Legacy only**]
  - Launch Video OpROM policy [Do not launch; UEFI only; **Legacy only**]
  - Other PCI device ROM priority [UEFI only; **Legacy OpROM**]

Security BIOS Setup Screen

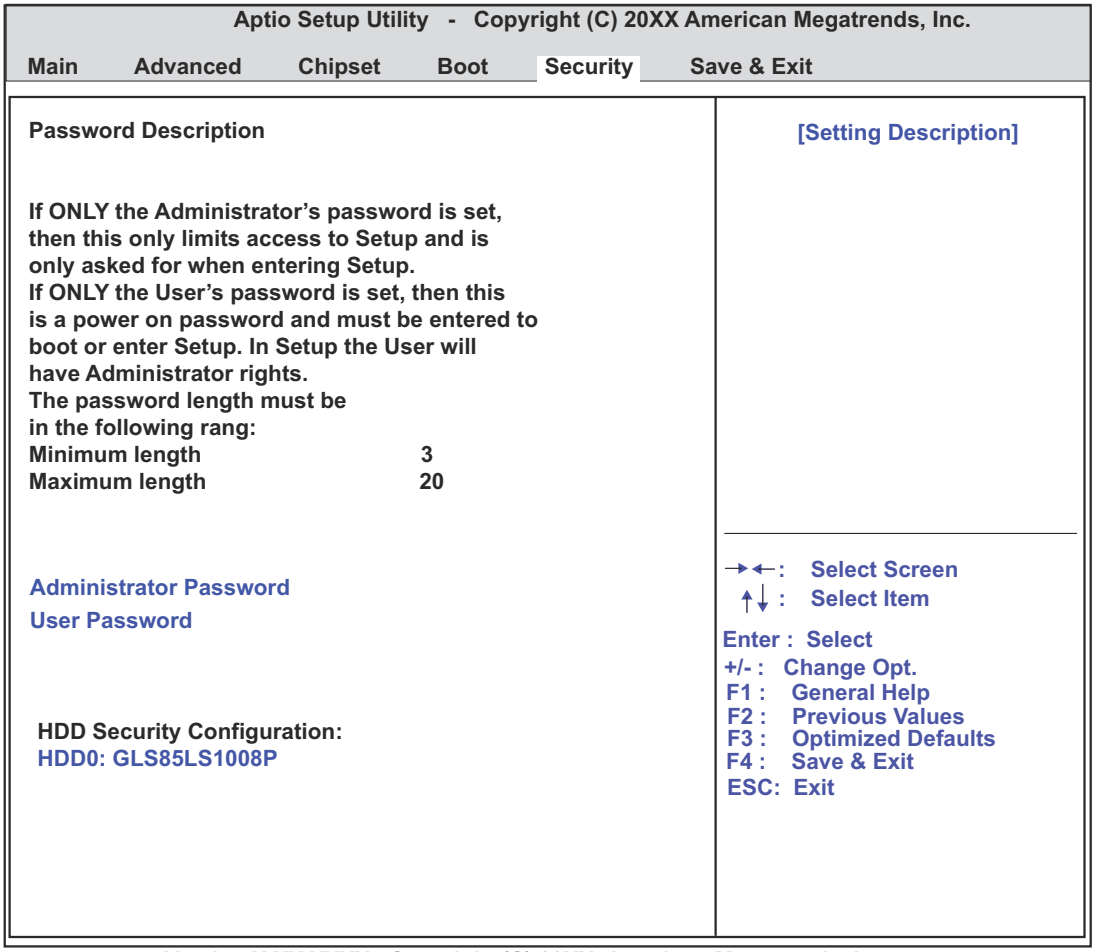

Figure 4-5. Security BIOS Setup Screen

- **Password Description**
  - Administrator Password [Create New Password]
  - User Password [Create New Password]
  - HDD Security Configuration:

- HDD0: GLS85LS1008P

  - HDD Password Description:

    Allows Access to Set, Modify and Clear HardDisk User and Master Passwords. User Password need to be installed for Enabling Security. Master Password can be modified only when successfully unlocked with Master Password in POST.

    HDD PASSWORD CONFIGURATION:

Security Supported	:	Yes / No
Security Enabled	:	Yes / No
Security Locked	:	Yes / No
Security Frozen	:	Yes / No
HDD User Pwd Status		Installed / Not Installed

    Set User Password

Save & Exit BIOS Setup Screen

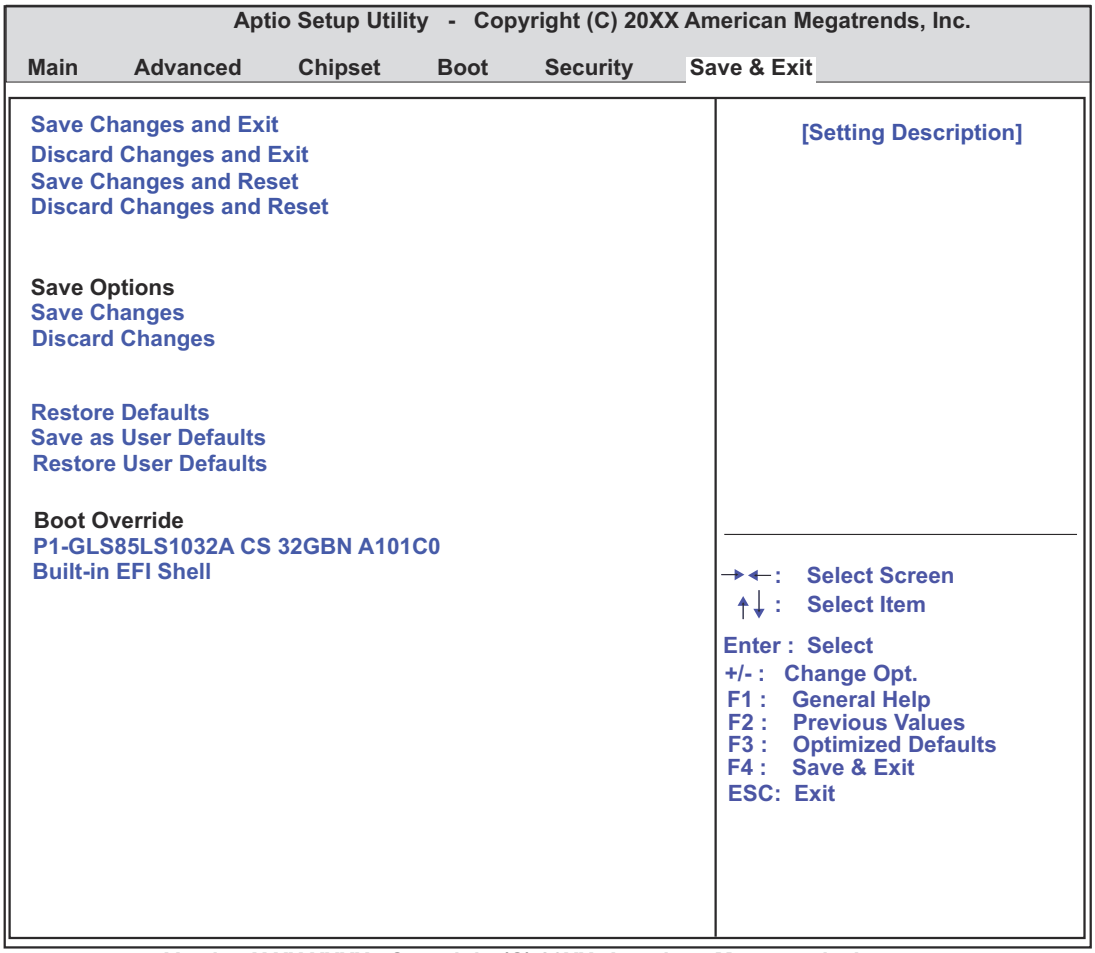

Figure 4-6. Save & Exit BIOS Setup Screen

- **Exit and Reset Options**
  - Save Changes and Exit
    - Save configuration and exit? [**Yes**; No]
  - Discard Changes and Exit
    - Quit without saving? [**Yes**; No] (ESC key can be used for this operation.)
  - Save Changes and Reset
    - Save configuration and reset? [**Yes**; No]
  - Discard Changes and Reset
    - Reset without saving? [**Yes**; No]

- **Save Options**
  - Save Changes
    - Save configuration? [**Yes**; No]
  - Discard Changes
    - Load Previous Values? [**Yes**; No]
  - Restore Defaults
    - Load Optimized Defaults? [**Yes**; No]
  - Save as User Defaults
    - Save configuration? [**Yes**; No]
  - Restore User Defaults
    - Restore User Defaults? [**Yes**; No]

- **Boot Override**
  - SATA PS: GLS85LS1008P CS XXGB
    - Save configuration and reset? [**Yes**; No]
  - Launch EFI Shell from filesystem device
    - Save configuration and reset? [**Yes**; No]

Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed below in Table A-1. Requests for support through the Ask an Expert are given the highest priority, and usually will be addressed within one working day.

- ADLINK's Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the Ampro By ADLINK web page at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

  ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called "My ADLINK" unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to My Stuff area where you can check status, update your request, and access other features.

- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1. Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	Contact us should you require any service or assistance. **ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

Table A-1. Technical Support Contact Information (Continued)

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1, B/D
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8625
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
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ADLINK Technology (Europe) GmbH
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Fax: +49-211-495-5557
Email: emea@adlinktech.com

ADLINK Technology, Inc. (French Liaison Office)
Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France
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Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
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神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 서울시 서초구 서초동 1506-25 한도 B/D 2 층
2F, Hando B/D, 1506-25, Seocho-Dong, Seocho-Gu,
Seoul 137-070, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre,
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: No. 1357, "Anupama", Sri Aurobindo Marg, 9th Cross,
JP Nagar Phase I, Bangalore - 560078, India
Tel: +91-80-65605817
Fax: +91-80-22443548
Email: india@adlinktech.com

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