DATA SHEET

NVIDIA Jetson TX2 / TX2i System-on-Module

Pascal GPU + ARMv8 + 8GB LPDDR4 + 32GB eMMC

NVIDIA Jetson Modules: TX2, TX2i

References to TX2 include (can be read as) TX2i except where explicitly noted.

Description

The NVIDIA® Jetson TX2 series System-on-Module (SOM) redefines possibility; a combination of performance, power efficiency, integrated deep learning capabilities and rich I/O remove the barriers to a new generation of products. The Jetson TX2 is ideal for many applications including (but not limited to): Intelligent Video Analytics (IVA), Drones, Robotics, Gaming Devices, Virtual Reality (VR), Augmented Reality (AR) and Portable Medical Devices. Superior performance, robust design and reduced complexity in system integration results in more advanced products getting to market faster.

The Jetson TX2 series module integrates:

- **256 core NVIDIA Pascal GPU**. Fully supports all modern graphics APIs, unified shaders and is GPU compute capable. The GPU supports all the same features as discrete NVIDIA GPUs, including extensive compute APIs and libraries including CUDA. Highly power optimized for best performance in embedded use cases.
- **ARMv8 (64-bit) Multi-Processor CPU Complex**. Two CPU clusters connected by a high-performance coherent interconnect fabric designed by NVIDIA; enables simultaneous operation of both CPU clusters for a true heterogeneous multi-processing (HMP) environment. The **Denver 2 (Dual-Core)** CPU clusters is optimized for higher single-thread performance; the ARM **Cortex-A57 MPCore (Quad-Core)** CPU clusters is better suited for multi-threaded applications and lighter loads.
- **Advanced HD Video Encoder**. Recording of 4K ultra-high-definition video at 60fps. Supports H.265 and H.264 BP/MP/HP/MVC, VP9 and VP8 encoding.
- **Advanced HD Video Decoder**. Playback of 4K ultra-high-definition video at 60fps with up to 12-bit pixels. Supports H.265, H.264, VP9, VP8 VC-1, MPEG-2, and MPEG-4 video standards.
- **Display Controller Subsystem**. Two multi-mode (eDP/DP/HDMI) outputs and up to 8-lanes of MIPI-DSI output. Multiple line pixel storage allows more memory-efficient scaling operations and pixel fetching. Hardware display surface rotation is also provided for bandwidth reduction in mobile applications.
- **128-bit Memory Controller**.128-bit DRAM interface providing high bandwidth LPDDR4 and ECC (**TX2i only**) support.
- **8GB LPDDR4 and 32 GB eMMC memory** integrated on the module
- **1.4Gpix/s Advanced image signal processing**: Hardware accelerated still-image and video capture path, with advanced ISP.
- **Audio Processing Engine**. Audio subsystem enables full hardware support for multi-channel audio over multiple interfaces.

Description	Jetson TX2 Series System-on-Module*	
	TX2	TX2i
Pascal GPU ◊		
256-core GPU | End-to-end lossless compression | Tile Caching | OpenGL® 4.6 | OpenGL® ES 3.2 | Vulkan® 1.0 | CUDA® 9.0		
Maximum Operating Frequency	1.12GHz	
CPU Complex ‡		
ARMv8 (64-bit) heterogeneous multi-processing (HMP) CPU architecture; two CPU clusters (6 processor cores) connected by a high-performance coherent interconnect fabric. NVIDIA Denver 2 (Dual-Core) Processor: L1 Cache: 128KB L1 instruction cache (I-cache) per core; 64KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB ARM® Cortex® -A57 MPCore (Quad-Core) Processor: L1 Cache: 48KB L1 instruction cache (I-cache) per core; 32KB L1 data cache (D-cache) per core | L2 Unified Cache: 2MB		
Maximum Operating Frequency per Core NVIDIA Denver 2 ARM Cortex-A57	 2.0GHz 2.0GHz	 1.95GHz 1.92GHz
HD Video & JPEG		
Video Decode(Number of Streams Supported): H.265 (†): Main 10, Main 8 H.265 (†): Main 444 H.264 (†): Baseline, Main, High H.264 (†): MVC Stereo (per view) VP9 (†): Profile 0 (8-bit) and 2 (10 and 12-bit) VP8: All MPEG1/2: Main MPEG4: SP/AP VC1: SP/MP/AP	 (2x) 2160p60 | (4x) 2160p30 | (7x) 1080p60 | (14x) 1080p30 2160p60 | (2x) 2160p30 | (3x) 1080p60 | (7x) 1080p30 (2x) 2160p60 | (4x) 2160p30 | (7x) 1080p60 | (14x) 1080p30 2160p60 | 2160p30 | 1080p60 | 1080p30 (2x) 2160p60 | (4x) 2160p30 | (7x) 1080p60 | (14x) 1080p30 2160p60 | (2x) 2160p30 | (4x) 1080p60 | (8x) 1080p30 2160p60 | (2x) 2160p30 | (4x) 1080p60 | (8x) 1080p30 (4x) 1080p60 | (8x) 1080p30 (2x) 1080p60 | (4x) 1080p30	
Video Encode (Number of Streams Supported): H.265 H.264: Baseline, Main, High WEBM VP9 WEBM VP8	 2160p60 | (3x) 2160p30 | (4x)1080p60 | (8x) 1080P30 2160p60 | (3x) 2160p30 | (7x) 1080p60 | (14x) 1080p30 2160p30 | (3x) 1080p60 | (7x) 1080p30 2160p30 | (3x) 1080p60 | (6x) 1080p30	
JPEG (Decode & Encode)	600 MP/sec	
Audio Subsystem		
Industry-standard High Definition Audio (HDA) controller provides a multi-channel audio path to the HDMI interface | 4 x I2S | DMIC | DSPK | 2 x I and Q baseband data channels | PDM in/out		
Display Controller Subsystem		
Support for DSI, HDMI, DP and eDP | Two multi-mode eDP/DP/HDMI outputs.		
Captive Panel		
MIPI-DSI (1.5Gbps/lane)	Max Resolution	Support for Single x4 or Dual x4 links | 2560x1600 at 60Hz
eDP 1.4 (HBR2 5.4Gbps)	Max Resolution	3840x2160 at 60Hz
External Display		
HDMI 2.0a/b (6Gbps)	Max Resolution	3840x2160 at 60Hz
DP 1.2a (HBR2 5.4 Gbps)	Max Resolution	3840x2160 at 60Hz
Imaging System		
Dedicated RAW to YUV processing engine process up to 1.4Gpix/s | MIPI CSI 2.0 up to 2.5Gbps (per lane) | Support for x4 and x2 configurations (up to 3 x4-lane or 6 x2-lane cameras)		
Clocks		
System clock: 38.4 MHz | Sleep clock: 32.768 KHz | Dynamic clock scaling and clock source selection		
Boot Sources		
Internal eMMC and USB (recovery mode)		

Description	Jetson TX2 Series System-on-Module*	
	TX2	**TX2i**
Security		
Secure memory with video protection region for protection of intermediate results | Configurable secure DRAM regions for code and data protection | Hardware acceleration for AES 128/192/256 encryption and decryption to be used for secure boot and multimedia Digital Rights Management (DRM) | Hardware acceleration for AES CMAC, SHA-1, SHA-256, SHA-384, and SHA-512 algorithms | 2048-bit RSA HW for PKC boot| HW Random number generator (RNG) SP800-90 | TrustZone technology support for DRAM, peripherals | SE/TSEC with side channel counter-measures for AES | RSA-3096 and ECC-512/521 supported via PKA		
Memory ††		
128-bit DRAM interface | Secure External Memory Access Using TrustZone Technology | System MMU | ECC (enabled by software for TX2i only)		
Memory Type	4ch x 32-bit LPDDR4	
Maximum Memory Bus Frequency (up to)	1866MHz	1600MHz
Memory Capacity	8GB	
Storage		
eMMC 5.1 Flash Storage		
Bus Width	8-bit	
Maximum Bus Frequency	200MHz (HS400)	
Storage Capacity	32GB	
Connectivity (TX2 only)		
WLAN		
Radio type	IEEE 802.11a/b/g/n/ac dual-band 2x2 MIMO	–
Maximum transfer rate	866.7Mbps	–
Bluetooth		
Version level	4.1	–
Maximum transfer rate	3MB/s	–
Networking		
10/100/1000 BASE-T Ethernet | IEEE 802.3u Media Access Controller (MAC) | Embedded memory		
Peripheral Interfaces Δ		
XHCI host controller with integrated PHY: (up to) 3 x USB 3.0, 3 x USB 2.0 | USB 3.0 device controller with integrated PHY | 5-lane PCIe: two x1 and one x4 controllers | SATA (1 port) | SD/MMC controller (supporting eMMC 5.1, SD 4.0, SDHOST 4.0 and SDIO 3.0): **1 x SD/SDIO at connector (TX2)**, **2 x SD/SDIO at connector (TX2i)** | 5 x UART | 3 x SPI | 8 x I^2C | 2 x CAN | 4 x I2S: support I^2S, RJM, LJM, PCM, TDM (multi-slot mode) | GPIOs		
Operating Requirements ♦		
Temperature Range	-25C – 80C	-40C to 85C
Module Power	7.5W (Max-Q) / 15W (Max-P)	10W (Max-Q) / 20W (Max-P)
Power Input	5.5V – 19.6V	9.0V – 19.6V
Applications		
Intelligent Video Analytics, Drones, Robotics, Industrial automation, Gaming, and more.		

* Refer to the software release feature list for current software support.

◊ GPU Maximum Operating Frequency: 1.3GHz supported in boost mode for Jetson TX2 and 1.23GHz for Jetson TX2i
Product is based on a published Khronos Specification and is expected to pass the Khronos Conformance Process. Current conformance status can be found at www.khronos.org/conformance.

‡ CPU Maximum Operating Frequency: 1-4 core = up to 2.0GHz; greater than 4-core = up to 1.4GHz

(†) For max supported number of instances: bitrate not to exceed 15 Mbps per HD stream (i.e., 1080p30), overall effective bitrate is less than or equal to 240 Mbps

†† Dependent on-board layout. Refer to *Jetson TX2/TX2i OEM Product Design Guide* for layout guidelines.

Δ Refer to *Jetson TX2/TX2i OEM Product Design Guide* and *Parker Series SoC Technical Reference Manual* to determine which peripheral interface options can be simultaneously exposed.

♦ Refer to the *Jetson TX2/TX2i OEM Product Design Guide* and the appropriate version of the Thermal Design Guide (either Jetson TX2 or TX2i) for evaluating product power and thermal solution requirements. See the software documentation for information on changing the default power mode (default: Max-P).

Revision History

Version	Date	Description
1.0	MAR 2018	Initial Release This document is being maintained as a separate instance from the Jetson TX2 Data Sheet. It supports both Jetson TX2 and Jetson TX2i modules. It is constructed so that those familiar with Jetson TX2 can easily locate any functional differences between the TX2 and TX2i modules

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1.0 Physical Description

The Jetson TX2 series SOM is a high performance, small-form factor device. It simplifies modular system design by mechanically isolating integrated components from external mechanical forces, standardizing thermal and mechanical interfaces, and exposing a comprehensive set of system and peripheral interfaces at a single board-to-board connector.

Core integrated components of the Jetson TX2 series module include:

- Tegra X2 (Parker Series SoC)
  - NVIDIA Pascal GPU
  - ARMv8 (64-bit) HMP CPU Complex
    - NVIDIA Denver 2 Dual-core CPU
    - ARM Cortex-A57 Quad-core CPU
- 8GB LPDDR4 memory
- 32GB eMMC 5.1 storage
- IEEE 802.11a/b/g/n/ac dual-band 2x2 WLAN and Bluetooth 4.1 combo chip (**TX2 only**)
- Gigabit Ethernet
- PMIC, regulators, power and voltage monitors
- Thermal Transfer Plate (TTP) primary thermal interface
- 400-pin board-to-board connector (exposes both high-speed and low-speed industry standard I/O)
- WLAN and BT antenna connectors (**TX2 only**)
- Temperature sensors
- Board ID EEPROM

Table 1 Module Interfaces at Connector

Category	Function
USB	USB 2.0 (3x)
	USB 3.0 (up to 3x)
PCIe	Control (x3), shared Wake
	PCIe (3 root ports)
SATA	SATA and device sleep control
Camera	CSI (6 x2) or (3 x4), control and clock
Display	eDP/DP/HDMI (2x)
	DSI (2 x4), display/backlight control
Audio	I2S (4x), control and clock
	Digital mic and speaker
SD Card	SD card or SDIO (**TX2i SD card and SDIO**)
LAN	Gigabit Ethernet

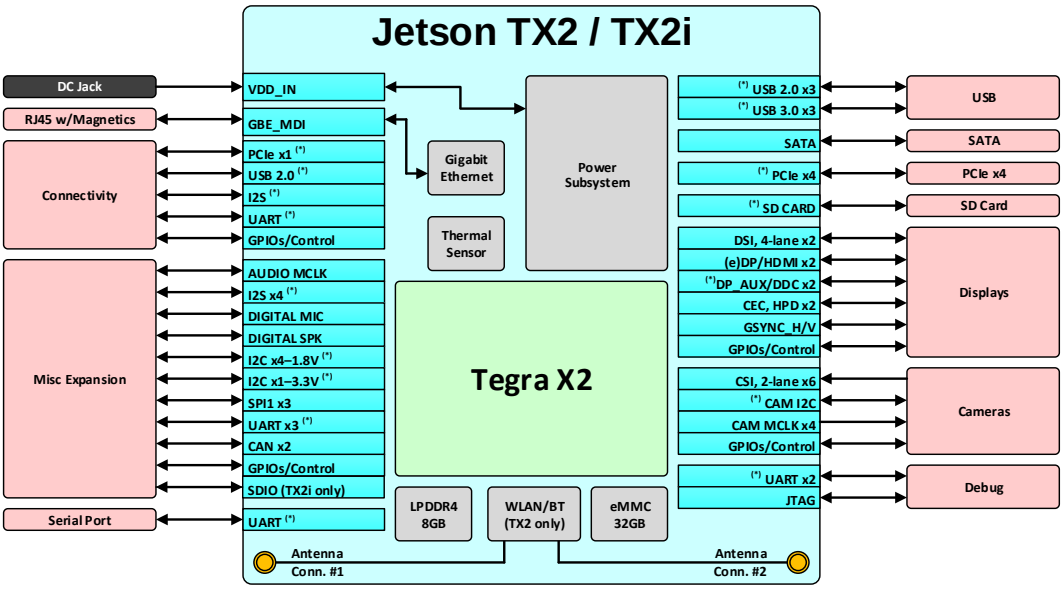
Category	Function
CAN	(2x)
I2C	(8x)
UART	(5x)
SPI	(3x)
WLAN/BT/Modem	SDIO/UART/I2S, control/handshake
Touch	Touch clock, interrupt, reset
Sensor	Control and interrupt
Fan	FAN PWM and Tach input
Debug	JTAG, UART
System	Power control, reset, alerts
Power	Main input

NOTE: TX2i modules support an SDIO interface in addition to the SD Card interface; TX2 modules only have a single SD card interface (any of these can support SD card or SDIO).

WLAN/BT/Modem are integrated on TX2; interfaces are available at connector for off-module use on TX2i

Not all interfaces listed above can be supported at the same time. See the *Jetson TX2/TX2i OEM Product Design Guide* for supported configurations and connection examples.

Figure 1 SOM Block Diagram – General Application



NOTE: (*) Not all interfaces shown above can be supported at the same time: some interfaces are shown in multiple locations to demonstrate usage (see Table 1 for the maximum number of each type of interface); USB 3.0, PCIe and SATA interfaces share lanes. See the *Jetson TX2/TX2i OEM Product Design Guide* for supported configurations and connection examples.

1.1 Connectivity (TX2 only)

NOTE: WLAN/BT/Modem are integrated on TX2; interfaces are available at connector for off-module use on TX2i

WLAN/Bluetooth integrated on the Jetson TX2 module supports:

- WLAN Ready
  - 2x2 MIMO
  - 802.11ac compliant (backwards compatible with legacy 802.11b/g/a/n devices)
- Bluetooth Ready
  - Bluetooth 4.1 ready (can connect to Bluetooth 4.1 enabled devices)
  - HIDP
  - Audio – A2DP (advanced audio distribution profile)
  - RFKILL

1.2 WLAN / BT Antenna Connectors (TX2 only)

NOTE: WLAN/BT/Modem are integrated on TX2; interfaces are available at connector for off-module use on TX2i

Male I-PEX antenna connectors for WLAN/ BT are located on the module. These support antennas with the following characteristics:

- Female I-PEX connector
- 2.4 GHz and 5 GHz frequency bands
- 50 Ω impedance

1.3 Thermal Characteristics

Jetson TX2 series modules were designed to be modular from both a functionality standpoint as well as a thermal standpoint. While it integrates several individual components the primary Jetson TX2 series module thermal interface is via a single Thermal Transfer Plate (TTP) that covers the top side. The TTP simplifies thermal design and integration with the system-level thermal solution. See the appropriate version of the Thermal Design Guide (either Jetson TX2 or TX2i) for complete details on the thermal evaluation and design process using Jetson TX2 series modules.

2.0 Functional Overview

The Jetson TX2 series SOM can be used in a wide variety of applications requiring varying performance metrics. To accommodate these varying conditions, frequencies and voltages are actively managed by Tegra Power and Thermal Management Software and influenced by workload.

2.1 Pascal GPU

NVIDIA introduced major improvements to performance and power efficiency with the new Pascal GPU architecture. The Jetson TX2 series module incorporates these same GPU architectural enhancements to further increase performance and reduce power consumption for computationally intensive workloads. The previous (Maxwell) GPU architecture introduced an all-new design for the Streaming Multiprocessor (SM); the Pascal GPU architecture continues to improve upon this SM design with the following enhancements:

- Simplified data path
- New SM scheduler architecture
- Improvements in scheduling and overlapped load/store instructions
- New arithmetic operations
- Improved support for large address spaces and page faulting capability

The Graphics Processing Cluster (GPC) is a dedicated hardware block for compute, rasterization, shading, and texturing; most of the GPU's core graphics functions are performed inside the GPC. It is comprised of multiple SM units and a Raster Engine. The SM unit creates, manages, schedules and executes instructions from many threads in parallel. Raster operators (ROPs) continue to be aligned with L2 cache slices and memory controllers. The SM geometry and pixel processing performance make it highly suitable for rendering advanced user interfaces and complex gaming applications; the power efficiency of the Pascal GPU enables this performance on devices with power-limited environments.

Each SM is partitioned into four separate processing blocks (referred to as SMPs), each SMP contains its own instruction buffer, scheduler and 32 CUDA cores. Inside each SMP, CUDA cores perform pixel/vertex/geometry shading and physics/compute calculations. Texture units perform texture filtering and load/store units fetch and save data to memory. Special Function Units (SFUs) handle transcendental and graphics interpolation instructions. Finally, the PolyMorph Engine handles vertex fetch, tessellation, viewport transform, attribute setup, and stream output.

Features:

- End-to-end lossless compression
- Tile Caching
- OpenGL 4.5, OpenGL ES 3.2, and Vulkan 1.0

  NOTE: Product is based on a published Khronos Specification and is expected to pass the Khronos Conformance Process. Current conformance status can be found at www.khronos.org/conformance.

- Adaptive Scalable Texture Compression (ATSC) LDR profile supported
- DirectX 12 compliant
- CUDA support

- Iterated blend, ROP OpenGL-ES blend modes
- 2D BLIT from 3D class avoids channel switch
- 2D color compression
- Constant color render SM bypass
- 2x, 4x, 8x MSAA with color and Z compression
- Non-power-of-2 and 3D textures, FP16 texture filtering
- FP16 shader support
- Geometry and Vertex attribute Instancing
- Parallel pixel processing
- Early-z reject: Fast rejection of occluded pixels acts as multiplier on pixel shader and texture performance while saving power and bandwidth
- Video protection region
- Power saving: Multiple levels of clock gating for linear scaling of power

2.2 CPU Complex

The CPU complex is comprised of two CPU clusters (6 processor cores total) in a coherent multi-processor configuration – MCPU cluster: Denver 2 (Dual-Core) Processor; BCPU cluster: ARM Cortex-A57 MPCore (Quad-Core) Processor. Both the Denver 2 and Cortex-A57 CPU clusters support ARMv8 executing both 64-bit Aarch64 code and 32-bit Aarch32 code, including legacy ARMv7 applications.

The two CPU clusters are connected by a high-performance coherent interconnect fabric designed by NVIDIA; this enables simultaneous operation of both CPU clusters (all 6 cores if required) for a true heterogeneous multi-processing (HMP) environment. The coherency mechanism allows tasks to be freely migrated, according to their performance needs, between the CPU cores with no overhead for manual cache flushing. The Denver 2 processor delivers significantly higher single-thread performance; achieved with dynamic code optimizations from NVIDIA that result in considerably more out-of-order operations and associated outstanding memory reads. The Cortex-A57 is better suited for multi-threaded applications and lighter loads.

Both CPU clusters interface to the MSelect FIFO via an AXI interface to decouple I/O traffic. MSelect allows an AXI master device to send traffic to the peripheral buses based on transaction address. The AXI/Xbar bridge enables early response on write transfers and full hardware hazard resolution to permit the maximum transaction throughput to MMIO.

2.2.1 NVIDIA Denver 2 (Dual-Core) Processor

Both cores in the Denver 2 processor are identical implementations of the ARMv8 architecture with NVIDIA optimizations. Each core includes 128KB Instruction (I-cache) and 64KB Data (D-cache) Level 1 caches. A 2MB L2 cache is shared by both cores. Denver 2 processor features include:

- Full implementation of the ARMv8 architecture
- NVIDIA Dynamic Code Optimization
- 7-wide Superscalar architecture
- Dynamic branch prediction with a Branch Target Buffer and Global History Buffer RAMs, a return stack buffer, and an indirect predictor.
- 128-entry 4-way-associative L1 instruction TLB with native support for 4KB page sizes.
- 256-entry 8-way-associative L1 data TLB with native support for 4KB, and 64KB pages sizes.
- 2048-entry 8-way set-associative accelerator TLB cache in each processor
- 128KB 4-way-associative parity protected L1 instruction cache
- 64KB 4-way-associative parity protected L1 data cache

- 2MB 16-way-associative ECC protected L2 cache shared by both Denver cores
- Embedded Trace Microcell (ETM) based on the ETMv4 architecture
- Performance Monitor Unit (PMU) based on the PMUv3 architecture
- Cross Trigger Interface (CTI) for multiprocessor debugging
- Cryptographic Engine for crypto function support
- Interface to an external Generic Interrupt Controller (vGIC-400)
- Support for power management with multiple power domains

2.2.2 ARM Cortex-A57 MPCore (Quad-Core) Processor

All four cores in the ARM Cortex-A57 are identical implementations of the ARMv8 architecture. Each core includes 48KB Instruction (I-cache) and 32KB Data (D-cache) Level 1 caches. A 2MB L2 cache is shared by all cores. Cortex-A57 processor features include:

- Full implementation of the ARMv8 architecture
- Superscalar, variable-length, out-of-order pipeline
- Dynamic branch prediction with Branch Target Buffer (BTB) and Global History Buffer RAMs, a return stack, and an indirect predictor
- 48-entry fully-associative L1 instruction TLB with native support for 4KB, 64KB, and 1MB page sizes.
- 32-entry fully-associative L1 data TLB with native support for 4KB, 64KB and 1MB pages sizes.
- 4-way set-associative unified 1024-entry Level 2 (L2) TLB in each processor
- Fixed 48KB parity protected L1 instruction cache and 32KB ECC protected L1 data cache
- A 2MB ECC protected L2 cache shared by all the Cortex-A57 cores
- Embedded Trace Microcell (ETM) based on the ETMv4 architecture
- Performance Monitor Unit (PMU) based on the PMUv3 architecture
- Cross Trigger Interface (CTI) for multiprocessor debugging
- Cryptographic Engine for crypto function support
- Interface to an external Generic Interrupt Controller (vGIC-400)
- Support for power management with multiple power domains
- Cortex-A57 Revision r1p3

2.3 Memory Controller

The Memory Controller (MC) maximizes memory utilization while providing minimum latency access for critical CPU requests. An arbiter is used to prioritize requests, optimizing memory access efficiency and utilization and minimizing system power consumption. The MC provides access to main memory for all internal devices. It provides an abstract view of memory to its clients via standardized interfaces, allowing the clients to ignore details of the memory hierarchy. It optimizes access to shared memory resources, balancing latency and efficiency to provide best system performance, based on programmable parameters. Structurally, the memory subsystem (MSS) consists of four major components:

- MSS backbone: routes requests from clients to the MC Hub and responses from MC Hub to the clients.
- MC Hub: receives client requests, performs SMMU translation, performs various security checks, and sends requests to the four MC Channels.
- MC Channels: row sorter/arbiter and DRAM controller.
- DRAMIO: channel-to-pad fabric, DRAM I/O pads, and PLLs.

Features:

- 128-bit memory interface supporting: LPDDR4 up to **3732 MT/s for TX2**, **3200 MT/s for TX2i**; delivering a peak bandwidth up to **59.7GB/s for TX2**, **28GB/s for TX2i**; implemented as four 32-bit channels with x16 sub-partitions
- Integrated ARM SMMU v2 (SMMU-500) IP with two stage translation to support virtualization
- Enhanced arbiter design for higher memory efficiency
- Support for encryption of traffic to/from DRAM to comply with SCSA security requirements
- 40-bit virtual addressing
- Generalized security apertures
- Variable transaction sizes based on the requests from the clients (e.g., one 64-byte transaction with variable dimensions, two 32-byte transactions with variable dimensions, etc.)
- Encryption
  - Uses AES-XTS with 128-bit key
  - Encrypts carveout regions (Microcode, TrustZone®, GSC, VPR)
- DRAM ECC (**enabled by software for TX2i only**)
  - Single Bit Error (SBE) correction, Double Bit Error (DBE) detection
  - Inline ECC (ECC stored in memory along with data)
  - 512 bytes in a DRAM page allocated for ECC
  - Hardware-assisted software demand scrub for correcting single-bit errors
- Dual CKE signals for dynamic power down per device
- Support for two DRAM ranks of unequal device densities
- Dynamic Entry/Exit from Self -Refresh and Power Down states

The MC is able to sustain high utilization over a very diverse mix of requests. For example, the MC is prioritized for bandwidth (BW) over latency for all multimedia blocks (the multimedia blocks have been architected to prefetch and pipeline their operations to increase latency tolerance); this enables the MC to optimize performance by coalescing, reordering, and grouping requests to minimize memory power. DRAM also has modes for saving power when it is either not being used, or during periods of specific types of use.

2.4 Image Signal Processor (ISP)

The ISP takes data from the VI or CSI block in raw Bayer format and processes it to YUV output. Advanced image processing is used to convert input to YUV data, and remove artifacts introduced by high-megapixel CMOS sensors, camera lens and color-space conversion.

Features:

- CSI Virtual Channel (VC) supports four VCs per CSI x4 brick
- SMMU ID support for guest OS virtualization
- Local Tone Map
- Bayer Histogram statistics for auto-exposure
- Bayer average map for auto white balance and auto-exposure
- Sharpness map for auto focus

2.5 Display Controller

The display controller complex contains two Serial Output Resources (SOR) which collects pixels from the output of a display pipeline, format/encode them to desired format and then streams to various output devices. The SOR consists of several individual resources which can be used to interface with different display devices such as HDMI or DP. A SOR can drive only a single device at any given time. In addition to SORs, two MIPI-DSI interfaces are available, which support up to 2 x 4-lane modes.

Features:

- 1/2/4 lane DP (DP 1.2a) and eDP (eDP 1.4)
- HDMI 2.0a/b
  - Support 8/12 bpc RGB and YUV444
  - Support 8/10/12 bpc YUV422
- Up to 36bpp* pixel depth on HDMI and DP; up to 24bpp* on DSI and eDP.

  NOTE: * (Resolution + Refresh Rate + Pixel Depth + Format) must be within specification limits to achieve support for desired pixel depth.
- ASSR scrambling for eDP panels
- On HDMI, multichannel audio from HDA controller, up to 8 channels 192 kHz 24-bit.
- 2x4 or 4x2 DSI
- Support frame-packed 3D stereo mode (not frame-sequential mode like dGPU)
- Support generic info-frame transmission
- Support HDMI Vendor Specific Info-frame (VSI) packet transmission
- Supported eDP 1.4 features:
  - Additional link rates (2.16, 2.43, 3.24, 4.32 Gbps)
  - Enhanced framing
  - Power sequencing
  - Reduced main voltage swing

2.6 High Definition (HD) Audio/Video Subsystem

The HD Audio-Video Subsystem uses a collection of functional blocks to off-load audio and video processing activities from the CPU subsystem, resulting in fast, fully concurrent, highly efficient operation.

This Subsystem is comprised of the following:

- Multi-Standard Video Decoder
- Multi-Standard Video Encoder
- JPG Processing Block
- Video Image Compositor (VIC)
- Audio Processing Engine (APE)

2.6.1 Multi-Standard Video Decoder

The video decoder accelerates video decode, supporting low resolution mobile content, Standard Definition (SD), High Definition (HD) and UltraHD (2160p, or “4k” video) profiles. The video decoder is designed to be extremely power efficient without sacrificing performance.

The video decoder communicates with the memory controller through the video DMA which supports a variety of memory format output options. For low power operations, the video decoder can operate at the lowest possible frequency while maintaining real-time decoding using dynamic frequency scaling techniques.

- Control and assist hardware audio decoding blocks
- Control and synchronize the video decode processor (NVDEC)

The following video standards are supported:

- H.265: Main10, Main, Main444
- WEBM VP9 and VP8
- H.264: Baseline, Main, High, Stereo SEI (half-res)
- VC-1: Advanced
- MPEG-4: Simple
- H.263: Profile 0
- DiVX: 4 / 5 / 6
- XviD Home Theater
- MPEG-2: MP

> **NOTE:** A/V codec, post-processing and containers support are subject to software support: refer to NVIDIA software documentation for current support.

2.6.2 Multi-Standard Video Encoder

The multi-standard video encoder enables full hardware acceleration of various encoding standards. It performs high quality video encoding operations for mobile applications such as video recording and video conferencing. The encode processor is designed to be extremely power efficient without sacrificing performance.

The following video standards are supported:

- H.265 Main Profile: I-frames and P-frames (No B-frames)
- H.264 Baseline/Main/High Profiles: IDR/I/P/B-frame support
- MVC
- WEBM: VP8,VP9
- MPEG4 (ME only)
- MPEG2 (ME only)
- VC1 (ME only): No B frame, no interlaced

> **NOTE:** A/V codec, post-processing and containers support are subject to software support: refer to NVIDIA software documentation for current support.

Features:

- Support for multi-stream simultaneous encoding, context switch at frame boundary
- Scalable performance (resolution and frame rate) for multi-stream encoding
- Recon Loop (DCT, Q, IDCT, IQ)
- Intra prediction
  - Periodic intra-frame insertion (camcorder)
  - Intra mode decision using all sub modes
- De-blocking
- CBR and VBR Rate control

- Entropy coding
- Timestamp for Audio/Video Sync
- Quantization post processing (QPP)
- Error resiliency
  - Bit based / MB based packetization for video telephony
  - Programmable Intra refresh
  - Context save restore
- Video telephony: sequence for eliminating bit rate spikes
- Input surface (90/180/270-degree) rotation and H/V flip
- CABAC and CAVLC conforming to H.264 standard
- MPEG-4 simple profile encoding tools
- MPEG-4 Short video header mode
- Motion estimation (ME) only mode
- Flexible rate control (programmable control processor to do rate control in software)

2.6.3 JPEG Processing

The JPEG processing block is responsible for JPEG (de)compression calculations (based on JPEG still image standard), image scaling, decoding (YUV420, YUV422H/V, YUV444, YUV400) and color space conversion (RGB to YUV).

Following are the input (encode) formats:

- Pixel width: 8bpc
- Subsample format: YUV420
- Resolution up to 16 x 16K
- Pixel pack format
  - Semi-planar for 420

Following are the output (decode) formats:

- Pixel width 8bpc
- Resolution up to 16K x 16K
- Pixel pack format
  - Semi-planar for YUV420
  - YUY2 for 422H/422V
  - Planar for YUV444

2.6.4 Video Image Compositor (VIC)

The Video Image Compositor implements various 2D image and video operations in a power-efficient manner. It handles various system UI scaling, blending and rotation operations, video post-processing functions needed during video playback, and advanced de-noising functions used for camera capture.

Features of the Video Image Compositor are:

- Color Decompression
- High-quality De-interlacing
- Inverse Teleciné

- Temporal Noise Reduction
  - High quality video playback
  - Reduces camera sensor noise
- Scaling
- Color Conversion
- Memory Format Conversion
- Blend/Composite
- 2D Bit BLIT operation
- Rotation

2.6.5 Audio Processing Engine (APE)

The Audio Processing Engine (APE) is a self-contained unit with dedicated audio clocking that enables Ultra Low Power (ULP) audio processing. Software based post processing effects enable the ability to implement custom audio algorithms.

Features:

- 96KB Audio RAM
- Low latency voice processing
- Audio Hub (AHUB)
  - 4 x I2S Stereo/TDM I/O
  - S/PDIF
  - DMIC
  - DSPK
- Multi-Channel IN/OUT
  - Digital Audio Mixer: 10-in/5-out
    - Up to 8 channels per stream
    - Simultaneous Multi-streams
    - Flexible stream routing
  - Multi-band Dynamic Range Compression (DRC)
    - Up to 3 bands
    - Customizable DRC curve with tunable knee points
    - Up to 192KHz, 32-bit sample, 8 channels
  - Parametric equalizer: up to 12 bands
  - Low latency sample rate conversion (SRC) and high quality asynchronous sample rate conversion (ASRC)

2.6.6 Tegra Security Controller (TSEC)

TSEC heavy-secure (HS) hardware is capable of authenticating its own code autonomously using its Secure Boot ROM and signature verification keys. The on-chip secure memory enables tamper resistant secure storage and transaction verification. TSEC implements a random number generator (RNG), and has a Falcon engine that supports AES-128b; no other cryptographic primitives or key sizes are supported. Two independent instruction queues (capable of holding up to 16 instructions) are used to provide encryption support for DRM schemes, including protected content encryption/ decryption.

Two instances of the TSEC controller (i.e., TSECA and TSECB) balance the performance requirements of increasingly demanding use cases.

Features:

- TSECA – performs GSC blob signing for NVDEC
- TSECA/B
  - Communicates with SE for any crypto acceleration, if required.
  - Side channel counter-measures for AES.
  - Dedicated video protection region in memory
    - Programmable in the memory controller
    - Extends security controller i-cache and d-cache
    - Only accessible by the Security Controller
    - Minimum size requirements avoid security exposure

2.7 Security Engine

A dedicated platform security engine supports secure boot, incorporates a NIST SP800-90 complaint random number generator (RNG) including built in ring oscillator based entropy source used to seed a deterministic random bit generator (DRBG), and a protected memory aperture for video use cases.

Features:

- Side channel attack prevention
- Encryption of memory traffic
- RSA PKC 2048-bit CMAC based boot support
- Support for multiple security domains throughout the control plane and peripheral bridges
- AES-128/192/256 encryption and decryption support
- SHA-1, SHA-224, SHA-256, SHA-384 and SHA-512 support
- RSA: 512, 768, 1024, 1536, 2048, 3072 and 4096-bit support
- ECC: 160, 192, 224, 256, 384, 512 and 521-bit support

2.8 Thermal Monitoring and Management

Thermal sensors are used to constantly monitor the temperature on the chip and generate the appropriate signal or interrupt based on the thermal event. Sensors are placed across the die to gauge the temperature of the whole chip. A thermal throttling controller centralizes management of the multiple on-chip thermal sensors.

The thermal throttling controller (SOC_THERM) performs:

- Thermal Sensor Management: handles access, capture and processing of data from the multiple thermal sensors.
- Thermal Event Detection: provides multiple software configurable thermal thresholds per sensor. Thermal threshold crossings can be configured to raise interrupts or trigger a hardware throttling response.
- Over-Current Detection: externally signaled event detection; configurable over-current (OC) input pins can be used to trigger throttle responses.
- Throttle Management and Prioritization: for each of the events that can trigger a throttle response, provides configuration of that throttling response; for example, a CPU temperature exceeding 95ºC could trigger a 50% throttling of the GPU clock. This block also enables prioritizing the throttling responses in the event multiple thermal or over-current events happen simultaneously.

3.0 Power and System Management

The Jetson TX2 series module was designed with ease of system integration in mind. Power is provided by a single DC input, it is supplied to the devices on board through a power management IC (PMIC) and dedicated voltage regulators; all internal module voltages and IO voltages are generated from this input. An optional back up battery can be attached to maintain the on system Real-Time Clock (RTC) when the main power is not present.

The Power Management Controller (PMC) interacts with an external Power Manager IC or PMU through side band signals. It incorporates power management features that enable both high speed operation and very low-power standby states. The PMC primarily controls voltage transitions for the Tegra processor as it transitions to/from different low power modes; it also acts as a slave receiving dedicated power/clock request signals as well as wake events from various sources (e.g., SPI, I2C, RTC) which can wake the Tegra processor from a deep sleep state. Tegra processors (with PMC support) are able to employ aggressive power-gating capabilities on idle modules. The PMC integrates specific logic to maintain defined states and control power domains (including signaling the external PMU to provide power) during sleep and deep sleep modes.

The PMC receives the primary chip reset event (from SYS_RESET_N) and generates various resets for: PMC, RTC and CAR. From the PMC provided reset, the Clock and Reset (CAR) controller generates resets for most of the blocks in the chip. The RTC module is maintained in the ‘always-on’ power domain, enabling support for both timer events and external triggers (e.g., key press or plugging in USB cable) when the system is in a low-power state.

3.1 Power Rails

VDD_IN must be supplied by the carrier board that the Jetson TX2 series module is designed to connect to. It must meet the required electrical specifications detailed in the Physical / Electrical Characteristics section. An optional back up battery can be connected to this input to maintain the Jetson TX2 series module RTC when VDD_IN is not present. When a backup cell is connected to the PMIC, the RTC will retain its contents and also can be configured to charge the backup cell.

NOTE: VDD_RTC is connected directly to the onboard PMIC. Backup cells must provide a voltage in the range 2.5V to 3.5V. These will be charged with a constant current (CC), constant voltage (CV) charger that can be configured between 2.5V and 3.5V CV output and 50uA to 800uA CC. The following backup cells may be attached to this pin:

- Super Capacitor (gold cap, double layer electrolytic)
- Standard capacitors (tantalum)
- Rechargeable Lithium Manganese cells

No additional IO voltage is required to be supplied to the module. All of the signals on the Jetson TX2 series module interfaces are referenced to on-module voltage rails. See the *Jetson TX2/TX2i OEM Product Design Guide* for details of connecting to each of the interfaces.

Table 26: Module Power Rails

Name	(V)	Description
VDD_IN	5.5 – 19.6 (**TX2**) 9.0 – 19.0 (**TX2i**)	Main power – Supplies PMIC and external supplies
VDD_RTC	1.65 – 5.5	Real-Time-Clock (RTC). Optionally used to provide back-up power for RTC.

Table 26: Module Control Signals

Name	Type	Description
VIN_PWR_BAD#	I	Carrier board indication to the module that the VDD_VIN power is not valid. Carrier board should de-assert this (drive high) when VDD_IN has reached its required voltage level and is stable. This prevents the module from powering up until the VDD_IN power is stable.
CARRIER_PWR_ON	O	Used as part of the power up sequence. The Jetson TX2 series module asserts this signal when it is safe for the carrier board to power up.

Name	Type	Description
RESET_IN#	I/O	System Reset driven from PMIC to carrier board for devices requiring full system reset. Also driven from carrier board to initiate full system reset (i.e. RESET button).
RESET_OUT#	I/O	Reset from PMIC (through diodes) to Tegra & eMMC reset pins. Driven from carrier board to force reset of Tegra & eMMC (not PMIC).
POWER_BTN#	I	Power button input to the Jetson TX2 from the carrier board. Used to initiate a system power-on.
SLEEP#	I	Sleep Request to the Jetson TX2 from the carrier board. A pull-up is present on the Jetson TX2.
CARRIER_STBY#	O	The Jetson TX2 drives this signal low when it is in the standby power state.
CHARGER_PRSNT#	I	Charger present. Can optionally be used to support auto-power-on where the Jetson TX2 platform will power-on when the main power source is connected instead of waiting for a power button press.
CHARGING#	I	Charger interrupt
BATT_OC	I/O	Battery over-current and thermal warning
WDT_TIME_OUT#	I	Watchdog timeout
FAN_PWM	O	Fan PWM
FAN_TACH	I	Fan tachometer
FORCE_RECOV#	I	Force recovery strap pin
SYS_WAKE#	I	Power button and SC7 wake interrupt
MOD_PWR_CFG_ID	O	Module power configuration identification. **Tied to GND on Jetson TX2i. Floating on Jetson TX2. Determines the power-on mechanism used to support both Jetson TX2 and TX2i.**

NOTE: Each Pulse Width Modulator (PWM) output supports a single independently programmable frequency divider and pulse width generator; the generated pulse is an n/256 duty cycle PWM clock. PWM outputs can run up to a maximum frequency of 102Mhz. PWM signals are useful for LCD contrast and brightness control, VCO-generated clocks and other analog voltage references where high precision is not required. See the *Parker Series SoC Technical Reference Manual* for PWM programming guidelines.

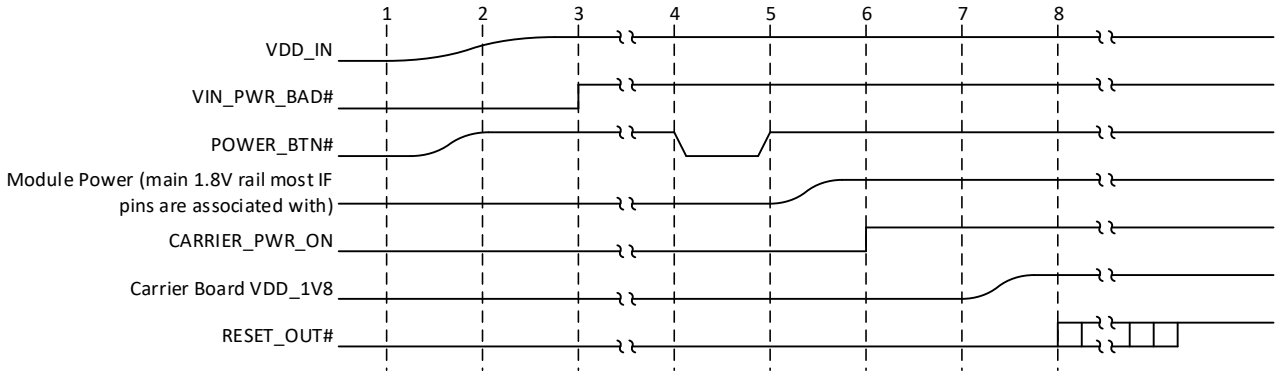
3.2 Power Sequencing

The Jetson TX2 series module and the product carrier board must be power sequenced properly to avoid potential damage to components on either the module or the carrier board system. The Jetson TX2 is powered before the main Carrier Board circuits. The CARRIER_PWR_ON signal is generated by the Jetson TX2 and passed to the Carrier Board to indicate that the Jetson TX2 is powered up and that the power up sequence for the Carrier Board circuits can begin. The following sections provide an overview of the power sequencing steps between the carrier board and Jetson TX2. Refer to the ***Jetson TX2/TX2i OEM Product Design Guide*** for system level details on the application of power, power sequencing and monitoring.

3.2.1 Power Up

During power up, the carrier board must wait until the signal CARRIER_PWR_ON is asserted from the Jetson TX2 before enabling its power. The Jetson TX2 will de-assert the RESET_OUT# signal to enable the complete system to boot.

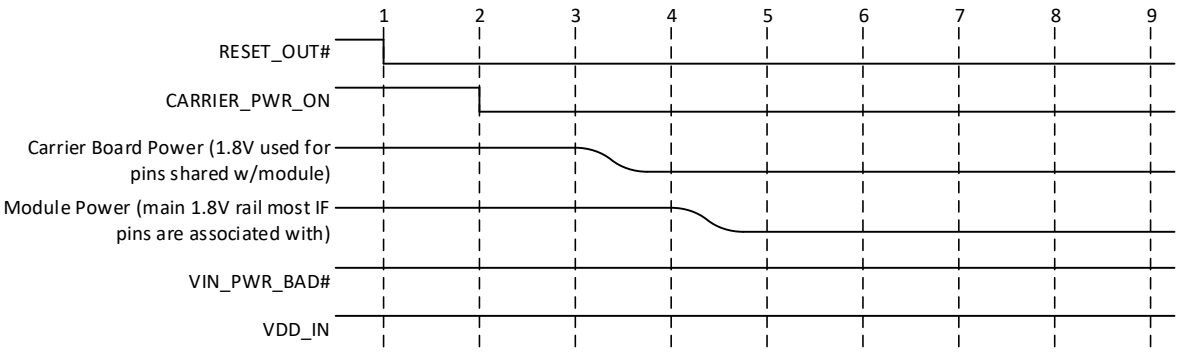
Figure 2 Power Up Sequence



3.2.2 Power Down

On receiving a Shutdown request the Jetson TX2 will assert the RESET_OUT# signal, allowing the carrier board to put any components into a known state. The CARRIER_PWR_ON signal will then be de-asserted to indicate to the carrier board to power down. The carrier board must disable its power at this point; the module will then disable its power and shut down. In order to meet the Power Down requirements, discharge circuitry is required. Refer to the ***Jetson TX2/TX2i OEM Product Design Guide*** for system level details on the application of power, power sequencing and monitoring.

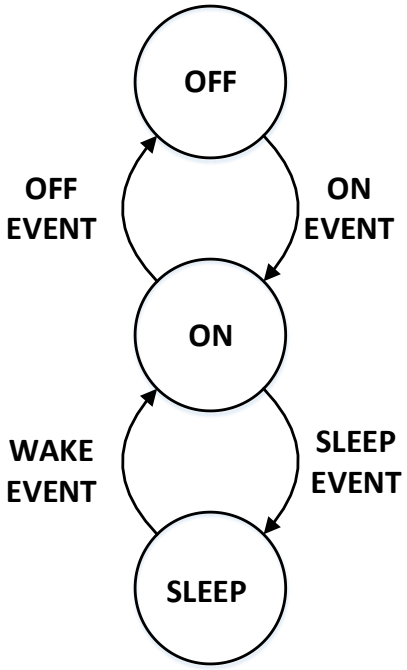
Figure 3 Power Down Sequence



3.3 Power States

The Jetson TX2 series module operates in 3 main power modes: OFF, ON and SLEEP. The module transitions between these states are based on various events from hardware or software. Figure 4 shows the transitions between these states.

Figure 4 Power State Diagram



3.3.1 ON State

The ON power state is entered from either OFF or SLEEP states. In this state the Jetson TX2 series module is fully functional and will operate normally. An ON event has to occur for a transition between OFF and ON states. The only ON EVENT currently used is a low to high transition on the POWER_BTN# pin. This must occur with VDD_IN connected to a power rail, and VIN_PWR_BAD# is asserted (at a logic1). The VIN_PWR_BAD# control is the carrier board indication to the Jetson TX2 series module to that the VDD_VIN power is not valid. The carrier board should de-assert this (drive high) when VDD_IN has reached its required voltage level and is stable. This prevents the Jetson TX2 series module from powering up until the VDD_IN power is stable.

> **NOTE:** The Jetson TX2 series module does include a system input (i.e., CHARGER_PRSNT#) that could enable the module to power on if asserted. For example, in the case of a system with a discharged battery state the Jetson TX2 series module may be required to monitor or control the charging settings. For more information on available signals and broader system usage, see the ***Jetson TX2/TX2i OEM Product Design Guide.***

When in the ON power state, the Jetson TX2 series module includes various design features to minimize the power when possible. These include such items as:

- Advanced Power Management IC (PMIC)
- On system Power Gating
- Advanced on chip Clock Gating
- Dynamic Voltage and Frequency Scaling (DVFS)
- Always on logic used to wake the system based on either a timer event or an external trigger (e.g., key press).
- Low power DRAM (LPDDR4)

3.3.2 OFF State

The OFF state is the default state when the system is not powered. It can only be entered from the ON state, through an OFF event. OFF Events are listed in the table below.

Table 27 OFF State Events

Event	Details	Preconditions
Power Button (10 second Press)	Keeping POWER_BTN# low for 7 seconds will power down the Jetson TX2 series module	In ON State
SW Shutdown	SW will initiate	ON state, SW operational
Thermal Shutdown	If the internal temperature of Jetson TX2 series module reaches an unsafe temperature, the HW is designed to initiate a shutdown	Any power state
Voltage Brown out	A voltage monitor circuit is implemented on the Jetson TX2 series module to indicate if the main DC input rail, VDD_IN, “droops” below an acceptable level. If VDD_IN drops below 5V, the HW is designed to initiate a shutdown.	Any power state

3.3.3 SLEEP State

The Sleep state can only be entered from the ON state. This state allows the Jetson TX2 series module to quickly resume to an operational state without performing a full boot sequence. In this state, the Jetson TX2 series module operates in low power with enough circuitry powered to allow the device to resume and re-enter the ON state. During this state the output signals from the Jetson TX2 series module are maintained at their logic level prior to entering the state (i.e. they do not change to a 0V level).

The SLEEP state can only be entered directly by SW. For example, operating within an OS, with no operations active for a certain time can trigger the OS to initiate a transition to the SLEEP state.

To Exit the SLEEP state a WAKE event must occur. WAKE events can occur from within the Jetson TX2 series module or from external devices through various pins on the Jetson TX2 series module connector. A full list is given in the table below.

Table 28 SLEEP State Events

Event	Details
RTC WAKE up	Timers within the Jetson TX2 series module can be programmed, on SLEEP entry. When these expire they will create a WAKE event to exit the SLEEP state.
Thermal Condition	If the Jetson TX2 series module internal temperature exceeds programmed hot and cold limits the system will be forced to wake up, so it can report and take appropriate action (shut down for example)
Low VDD_IN	If VDD_IN voltage drops below a minimum voltage threshold, then the system can be woken up to initiate a graceful shutdown.
USB VBUS detection	If VBUS is applied to the system (USB cable attached) then the device can be configured to Wake and enumerate
SD Card detect	The Card detect pin may be configured to enable the system to wake.
On module WLAN Wake	WLAN can be configured to Wake up the system.
On module Bluetooth Wake	Bluetooth events can also trigger a system Wake.
Module connector Interface WAKE signal	Programmable signals on the Jetson TX2 series module connector.

Table 29 Programmable Interface WAKE Events

Event (Reference Design Signal)	Jetson TX2/TX2i Pin Assigned	Wake #
PCIe Wake Request (PEX_WAKE#)	PEX_WAKE#	1
Bluetooth Wake AP (BT2_WAKE_AP – Secondary)	GPIO13_BT_WAKE_AP	8
Wi-Fi Wake AP (WIFI_WAKE_AP – Secondary)	GPIO10_WIFI_WAKE_AP	9

Event (Reference Design Signal)	Jetson TX2/TX2i Pin Assigned	Wake #
Thermal/Over-current Warning	RSVD (C8)	10
Audio Codec Interrupt (AUD_INT_L)	GPIO20_AUD_INT	12
DP 0 Hot Plug Detect (DP_AUX_CH0_HPD)	DP0_HPD	19
HDMI Consumer Electronic Control (HDMI_CEC)	HDMI_CEC	20
DP 1 Hot Plug Detect (DP_AUX_CH0_HPD)	DP1_HPD	21
Camera Vertical Sync (CAM_VSYNC)	CAM_VSYNC	23
POWER_BTN#	POWER_BTN#	29
Motion Interrupt (MOTION_INT)	GPIO9_MOTION_INT	46
CAN 1 Error (CAN1_ERR)	CAN1_ERR	47
CAN Wake (CAN_WAKE)	CAN_WAKE	48
CAN 0 Error (CAN0_ERR)	CAN0_ERR	49
Touch Interrupt (TOUCH_INT)	GPIO6_TOUCH_INT	51
USB VBUS Detect (USB_VBUS_DET)	USB0_VBUS_DET	53
GPIO Expansion 0 Interrupt (GPIO_EXP0_INT)	GPIO_EXP0_INT	54
Modem Wake AP (MDM_WAKE_AP)	GPIO16_MDM_WAKE_AP	55
Battery Low (BATLOW#)	BATLOW#	56
GPIO Expansion 1 Interrupt (GPIO_EXP1_INT)	GPIO_EXP1_INT	58
USB Vbus Enable 0 (USB_VBUS_EN0)	USB_VBUS_EN0	61
USB Vbus Enable 1 (USB_VBUS_EN1)	USB_VBUS_EN1	62
Ambient Light Proximity Interrupt (ALS_PROX_INT)	GPIO8_ALS_PROX_INT	63
Modem Coldboot (MDM_COLDBOOT)	GPIO18_MDM_COLDBOOT	64
Force Recovery (FORCE_RECOV#)	FORCE_RECOV#	67
Sleep (SLEEP_L)	SLEEP#	68

3.4 Clocks

The Jetson TX2 series module requires no external clocks for operation, all system clocks are generated within the module; this includes a low power 32.768kHz system clock. An on-module 38.4MHz oscillator is used as the reference clock for most PLLs in the system. See the *Jetson TX2/TX2i OEM Product Design Guide* for connection examples and the *Parker Series SoC Technical Reference Manual* for a complete description of clock controls and programing guidelines.

3.5 WLAN Power States (TX2 only)

NOTE: Not supported on TX2i

The integrated dual band WLAN supports both STA Mode and P2P Powersave States.

3.5.1 STA Mode

- PM0: No powersave, always on.
- PM1: Legacy 802.11 powersave. STA must indicate to the AP that it is entering into powersave by setting the PM bit in a data packet. Upon acknowledgement from the AP it can go into powersave. STA must wake up periodically (at period=DTIM) to check AID in the TIM map. If AID is set, STA will use a PS-Poll packet to fetch buffered packets (one PS-Poll per buffered packet). This is an inefficient mechanism as the traffic will tend to be bursty.
- PM2: Vendor implementation. In PM2 mode, whenever there is a traffic (either Tx or Rx), the DUT will come out of powersave and remain there until packet exchanges have ceased for a minimum idle period (typically 200ms). When there is traffic, PM2 will operate nearly as well as PM0 mode, with almost no PS related latency. When there is no traffic, PM2 will be similar to PM1 powersave.

3.5.2 P2P Group-owner Powersave States

- Opportunistic Power Save (OPS): OPS allows the P2P Group Owner to save power when all associated clients are in a sleep state. P2P Power Management protocol defines an availability period “CTWindow” (Client Traffic Window), during which a P2P Group Owner is present. P2P Clients are allowed to transmit during CTWindow period. If at the end of the CTWindow all associated P2P Clients are in a sleep state, the P2P Group Owner is permitted to sleep until the next Beacon time. However, if any P2P Client remains in active mode at the end of the CTWindow the P2P Group Owner must remain awake until the next Beacon time.

  To change OPS mode:

  - Use the wpa_cli utility to issue the command “p2p_set ctwindow <value>”
  - Where ‘value’ is CTwindow in ms
  - Use the wpa_cli utility to issue the command “p2p_set opps <value>”
  - Where ‘value’ 1/0 enables/disables OPS respectively (this must be issued every time the CTwindow is changed in order to be reflected in the firmware)
- Notice-of-Absence (NoA): NoA is similar to the Opportunistic Power Save protocol. For NoA, GO defines absence periods with a signaling element included in Beacon frames and probe responses.

  To configure NoA:

  - Use the wpa_cli utility to issue the command “p2p_set noa <count, start, duration>”
  - Where duration is the length of each absence period, start time is the start time of the first absence period (after the current beacon frame), and count is the number of absence periods to schedule during the current NoA.

3.6 Bluetooth Power States (TX2 only)

NOTE: Not supported on TX2i

The integrated a Bluetooth (BT) controller includes the following power states:

- Active: this is the default state. No power savings.
- LP: this is the power saving state. The BT chip will go into low power mode, and will wake on traffic.

To change the mode: Assert/deassert the ext_wake GPIO to put the chip in Active or LP mode.

The BT controller also includes a wake-on-BT function. When it receives data, the chip will assert Host_wake GPIO. The module, depending on its state, can treat it as a wake interrupt or info GPIO.

4.0 Interface and Signal Descriptions

This section describes device signals. Additional alternate use signals are listed in the pinmux spreadsheet supporting this module. Signals are arranged in functional groups according to their associated interface.

4.1 Storage Controllers and Interfaces

4.1.1 SD/eMMC Controller

Standard	Notes
SD Specifications, Part A2, SD Host Controller Standard Specification, Version 4.1	
SD Specifications, Part 1, Physical Layer Specification, Version 4.2	
SD Specification, Part 1, eSD (Embedded SD) Addendum, Version 2.10	
SD Specifications, Part E1, SDIO Specification Version, 4.1	Support for SD 4.0 Specification without UHS-II
JEDEC Standard, Embedded Multimedia Card (e•MMC) Electrical Standard 5.1	JESD84-B51

The SecureDigital (SD)/Embedded MultiMediaCard (eMMC) controller is capable of interfacing to an external SD card or SDIO device, and provides the interface for the on-module eMMC and WLAN. It has a direct memory controller interface and is capable of initiating data transfers between system memory and an external card or device. It also has an APB slave interface to access its configuration registers. To access the on-chip System RAM for MicroBoot, the SD/MMC controller relies on the path to System RAM in the memory controller.

Features:

- 8-bit data interface to on-module eMMC
- 4-bit data interface: **TX2 – on-module WLAN/BT**; **TX2i – supports additional SD/SDIO interface at connector**
- 4-bit data interface for SD cards
- Supports card interrupts for SD cards (1/4/8-bit SD modes) and SDIO devices
- Supports read wait control and suspend/resume operation for SD cards
- Supports FIFO overrun and underrun condition by stopping SD clock
- Supports addressing larger capacity SD 3.0 or SD-XC cards up to 2 TB.

The Jetson TX2 series module brings out a single instance of this controller to the board-to-board connector: the SDCARD interface is intended for supporting an SD Card socket or compatible SDIO device. The SD/SDIO controllers support Default and High-Speed modes as well as the High and Low voltage ranges.

NOTE: To avoid potential CRC error in SDR50 mode set UHS_MODEL_SEL to SDR104 in SDMMC controller even though card is in SDR50 mode.

Table 30 SD/MMC Controller I/O Capabilities

Controller	Bus Width	Supported Voltages (V)	I/O bus clock (MHz)	Maximum Bandwidth (MBps)	Notes
SDCARD	4	3.3/1.8	208	104	SD (Primary SD Card). Alternate use SDIO interface.
SDIO	4	1.8	208	104	**TX2 – Used for WLAN/BT** **TX2i – Available for SD/SDIO at module pins**

Table 31 SD/SDIO Signal Descriptions

Signal Name	Type	Description
SDCARD_CLK	O	SD/SDIO Card Clock: Connect to CLK pin of device or socket
SDCARD_CMD	I/O	SD/SDIO Command: Connect to CMD pin of device/socket
SDCARD_D[3:0]	I/O	SD/SDIO Data: Connect to Data pins of device or socket
SDCARD_CD#	I	SDIO Card Detect: Connect to CD/C_DETECT pin on socket if required.
SDCARD_WP	I	SDIO Write Protect: Connect to WP/WR_PROTECT pin on socket if required.
SDIO_RST#	O	SDIO Reset: Connect to reset line on SDIO peripheral/connector.
SDCARD_PWR_EN	O	SD Supply/Load Switch Enable: Connect to enable of supply/load switch supplying VDD on SD Card socket.
SDIO_CLK	O	**TX2i only** – SDIO/SD Card Clock: Connect to CLK pin of device or socket
SDIO_CMD	I/O	**TX2i only** – SDIO/SDMMC Command: Connect to CMD pin of device/socket
SDIO_D[3:0]	I/O	**TX2i only** – SDIO/SDMMC Data: Connect to Data pins of device or socket

4.1.2 Serial ATA (SATA) Controller

Standard	Notes
Serial ATA Revision 3.1	Including all errata, ENC, and TP, except DHU (direct head unload)
Serial ATA Advanced Host Controller Interface (AHCI) Specification, Rev 1.3.1	

NOTE: See the ***Jetson TX2/TX2i OEM Product Design Guide*** for supported USB 3.0/PCIe/SATA configurations and connection examples.

The SATA controller enables a control path from the module to an external SATA device. A SSD / HDD / ODD drive can be connected. Controller can support the maximum throughput of a Gen 2 drive.

Features:

- Sleep support
  - Partial and slumber link power management
  - Host initiated power management

    NOTE: Device Initiated Power Management (DIPM) is not supported, device sleep cannot be enabled for drives that support only DIPM
- Port multiplier support
  - Command based switching (CBS)
- Supported Cables and connectors
  - Standard internal connector
  - Internal micro connector
  - Internal slimline connector
  - mSATA connector
  - BGA SSD interface
  - Not supported: External connector (eSATA), USM, Internal LIF-SATA

Table 32 SATA Signal Descriptions

Signal Name	Type	Description
SATA _TX+/–	I	Differential Transmit Data Pair: Connect to SATA+/– pins of SATA device/connector
SATA _RX+/–	O	Differential Receive Data Pair: Connect to SATA+/– pins of SATA device/connector
SATA_DEV_SLP	O	SATA Device Sleep: Connect through level shifter to matching pin on device or connector

4.2 USB Interfaces

Standard	Notes
Universal Serial Bus Specification Revision 3.0	Refer to specification for related interface timing details.
Universal Serial Bus Specification Revision 2.0	USB Battery Charging Specification, version 1.2; including Data Contact Detect protocol Modes: Host and Device Speeds: Low, Full, and High Refer to specification for related interface timing details.
Enhanced Host Controller Interface Specification for Universal Serial Bus revision 1.0	Refer to specification for related interface timing details.

NOTE: See the ***Jetson TX2/TX2i OEM Product Design Guide*** for supported USB 3.0/PCIe/SATA configurations and connection examples.

The Jetson TX2 series module integrates one xHCI host controller supporting (up to) three USB 2.0 ports and three USB 3.0 ports; of these six ports, one can be USB 3.0 OTG or USB 2.0 OTG while the rest are host mode only ports.

Features:

- Detect wake events
- VBUS and ID pin assertion/detection status via dedicated sideband signals
- Battery Charging
  - Supports standard and charging downstream port identification control when programmed as host/downstream ports
  - Supports charging port detection reporting as when programmed device/upstream ports
- On-the-Go (OTG)
  - SuperSpeed and HighSpeed/FullSpeed device only – LowSpeed not supported
  - Supports OTG SuperSpeed role swap protocol (RSP) and HighSpeed host negotiation protocol (HNP)
  - Supports Session request protocol (SRP)
  - Does not support attach detection protocol (ADP)

4.2.1 USB 2.0

USB 2.0 ports operate in USB 2.0 High Speed mode (up to 480Mb/s) when connecting directly to a USB 2.0 peripheral and USB 1.1 Full and Low Speed modes (up to 12Mb/s) when connecting directly to a USB 1.1 peripheral. Supports software-initiated link power management.

Table 33 USB 2.0 Signals

Signal	Type	Description
USB[2:0]_D+/–	I/O	Differential USB Data
USB[1:0]_EN_OC#	I/O	USB enable and over-current indication

Signal	Type	Description
USB0_OTG_ID	I	USB identification
USB0_VBUS_DET	I	VBus Detect

4.2.2 USB 3.0

USB 3.0 ports only operate in USB 3.0 Super Speed mode (up to 5Gb/s). Supports hardware and software-initiated link power management.

Table 34 USB 3.0 Signals

Signal	Type	Description
USB_SS0_RX+/– (USB 3.0 port #0) PEX_RFU_RX+/- (USB 3.0 port #1) USB_SS1_RX+/– (USB 3.0 port #2)	I	USB 3.0 Differential Receive Data Pairs: Connect to USB 3.0 connectors, Hubs or other devices on the PCB.
USB_SS0_TX+/– (USB 3.0 port #0) PEX_RFU_TX+/- (USB 3.0 port #1) USB_SS1_TX+/– (USB 3.0 port #2)	O	USB 3.0 Differential Transmit Data Pairs: Connect to USB 3.0 connectors, Hubs or other devices on the PCB.

4.3 PCI Express (PCIe) Interface

Standard	Notes
PCI Express Base Specification Revision 2.0	The Jetson TX2 series module meets the timing requirements for the Gen2 (5.0 GT/s) data rates. Refer to specification for complete interface timing details. Although NVIDIA validates that the module design complies with the PCIe specification, PCIe software support may be limited.

NOTE: See the ***Jetson TX2/TX2i OEM Product Design Guide*** for supported USB 3.0/PCIe/SATA configurations and connection examples.

Jetson TX2 series module do not support PCIe devices that cannot return all bytes corresponding to the byte enables asserted on the bus per Section 2.2.5 of the PCIe base specification - for byte enables, a value of 1b indicates that the corresponding byte of data must be read at the completer; if such non-conforming devices are used, software should limit its accesses to DWORD-aligned addresses only.

The Jetson TX2 series module integrates a x5 lane PCIe® bridge to enable a control path from the module to external PCIe devices with support for up to 5 lanes, and 3 separate interfaces. All three interfaces support upstream and downstream AXI that serves as the control path from the Jetson TX2 series module to the external PCIe device

Features:

- Configurations and Link Speed
  - x4 lane configurations
    - Supports x4, x2, and x1 configurations with conventional PCIe interface
    - Supports lane reversal for x4 and lane flipping for x2 and x1
    - Supports polarity inversion
    - Supports Gen1 and Gen2 link speed
    - Supports dynamic link speed and lane width change
  - x1 lane configurations
    - Supports polarity inversion
    - Supports Gen1 and Gen2 link speed for conventional PCIe
  - Possible configurations
    - x4 + x1
    - x2 + x1 + x1
    - x1 + x1 + x1

- Dedicated PEX_RST#, PEX_CLK and PEX_CLKREQ# signals for each PCIe interface
- One PEX_WAKE# signal
- PCIe Transactions
  - Supports 128-byte maximum payload size
  - Supports 64-bit address
  - Supports completion timeout with configurable timeout range
  - Does not support TLP prefixes or ECRC
  - Message Signaled Interrupts
  - Transaction ordering and coherency
    - Supports PCIE transaction ordering rules
    - Supports relaxed ordering
    - Supports No Snoop bit forwarding for upstream/DMA requests
    - Does not support ID-based ordering

Table 35 PCIe Signal Descriptions

Signal	Type	Description
PEX_WAKE#	I	PCI Express Wake This signal is used as the PCI Express defined WAKE# signal. When asserted by a PCI Express device, it is a request that system power be restored. No interrupt or other consequences result from the assertion of this signal.
PCIe Interface #0		
PEX0_REFCLK+/–	O	Differential Reference Clocks. PEX0_REFCLK is associated with PCIe interface #0.
PEX_RFU_RX+/– (Lane 3) PEX2_RX+/– (Lane 2) USB_SS1_RX+/– (Lane 1) PEX0_RX+/– (Lane 0)	I	Differential Receive Data Lanes, associated with PCIe interface #0.
PEX_RFU_TX+/– (Lane 3) PEX2_TX+/– (Lane 2) USB_SS1_TX+/– (Lane 1) PEX0_TX+/– (Lane 0)	O	Differential Transmit Data Lanes, associated with PCIe interface #0.
PEX0_CLKREQ#	I/O	PCI Express Reference Clock Request This signal is used by a PCI Express device to indicate it needs the PEX0_REFCLK+ and PEX0_REFCLK- to actively drive reference clock. PEX0_CLKREQ# is associated with PCIe interface #0.
PEX0_RST#	O	PCI Express Reset This signal provides a reset signal to all the PCI Express links. It must be asserted 100 ms after the power to the PCI Express slots has stabilized. PEX0_RST# is associated with PCIe interface #0.
PCIe Interface #1		
PEX2_REFCLK+/–	O	Differential Reference Clocks. PEX2_REFCLK is associated with PCIe interface #1.
PEX2_RX+/– (Lane 0)	I	Differential Receive Data Lane, associated with PCIe interface #1.
PEX2_TX+/– (Lane 0)	O	Differential Transmit Data Lane, associated with PCIe interface #1.
PEX2_CLKREQ#	I/O	PCI Express Reference Clock Request This signal is used by a PCI Express device to indicate it needs the PEX2_REFCLK+ and PEX2_REFCLK- to actively drive reference clock. PEX2_CLKREQ# is associated with PCIe interface #1.

Signal	Type	Description
PEX2_RST#	O	PCI Express Reset This signal provides a reset signal to all the PCI Express links. It must be asserted 100 ms after the power to the PCI Express slots has stabilized. PEX1_RST# is associated with PCIe interface #1.
PCIe Interface #2		
PEX1_REFCLK+/–	O	Differential Reference Clocks. PEX1_REFCLK is associated with PCIe interface #2.
PEX1_RX+/– (Lane 0)	I	Differential Receive Data Lanes, associated with PCIe interface #2.
PEX1_TX+/– (Lane 0)	O	Differential Transmit Data Lanes, associated with PCIe interface #2.
PEX1_CLKREQ#	I/O	PCI Express Reference Clock Request This signal is used by a PCI Express device to indicate it needs the PEX1_REFCLK+ and PEX1_REFCLK- to actively drive reference clock. PEX1_CLKREQ# is associated with PCIe interface #2.
PEX1_RST#	O	PCI Express Reset This signal provides a reset signal to all the PCI Express links. It must be asserted 100 ms after the power to the PCI Express slots has stabilized. PEX1_RST# is associated with PCIe interface #2.

4.4 Display Interfaces

The Jetson TX2 series module Display Controller Complex integrates two MIPI-DSI interfaces and two Serial Output Resources (SOR) supporting HDMI, DP or eDP output.

4.4.1 MIPI Display Serial Interface (DSI)

Standard	Notes
MIPI D-PHY 1.2	
MIPI DSI 1.0.1	Mandatory features

The MIPI Display Serial Interface (DSI) provides the means of transferring pixel data from the display controller internal to the Jetson TX2 series module, to an external third-party LCD module. The Jetson TX2 series module supports eight total MIPI DSI data lanes. Each data lane has a peak bandwidth up to 1.5Gbps. To support large resolution panels, the Jetson TX2 series module provides a mechanism to drive a single video source over multiple DSI links in a Dual DSI mode.

The following configurations are supported:

- Single Display (Dual DSI Mode): DSI-A (1x4) + DSI-C (1x4)
- Two Displays: DSI-A (1x4) to one display, DSI-C (1x4) to a second display

Features:

- PHY Layer
  - Start / End of Transmission. Other out-of-band signaling
  - Per DSI interface: 1 Clock Lane; up to 4 Data Lanes
  - Supports dual link operation in 2x4 configurations for asymmetrical/symmetrical split in both left-right side or odd-even group split schemes.
  - Maximum HS transmit rate 1.5Gbps
  - Maximum 10MHz LP receive rate
- Lane Management Layer with Distributor
- Protocol Layer with Packet Constructor

- Command Mode (One-shot) with Host and/or display controller as master
- Clocks
  - Bit Clock : Serial data stream bit-rate clock
  - Byte Clock : Lane Management Layer Byte-rate clock
  - Application Clock: Protocol Layer Byte-rate clock.
- Error Detection / Correction
  - ECC generation for packet Headers
  - Checksum generation for Long Packets
- Error recovery
- High Speed Transmit timer
- Low Power Receive timer
- Turnaround Acknowledge Timeout

Table 36 MIPI DSI Signal Descriptions

Name	Type	Description
DSI[3:0]_CK+/–	O	DSI Differential Clocks: Connect to CLKn & CLKp pins of receiver
DSI[3:0]_D[1:0]+/–	O	DSI Differential Data Lanes: Connect to Dn & Dp pins of DSI display
LCD_TE	I	LCD Tearing Effect: Connect to LCD Tearing Effect pin if supported
LCD_BKLT_EN	O	LCD Backlight Enable: Connect to LCD backlight solution enable if supported
LCD[1:0]_BKLT_PWM	O	LCD Backlight Pulse Width Modulation: Connect to LCD backlight solution PWM input if supported
LCD_VDD_EN	O	LCD Power Enable: .Connect as necessary to enable appropriate Display power supply(ies)

NOTE: Each Pulse Width Modulator (PWM) output supports a single independently programmable frequency divider and pulse width generator; the generated pulse is an n/256 duty cycle PWM clock. PWM outputs can run up to a maximum frequency of 102Mhz. PWM signals are useful for LCD contrast and brightness control, VCO-generated clocks and other analog voltage references where high precision is not required. See the ***Parker Series SoC Technical Reference Manual*** for PWM programming guidelines.

4.4.2 High-Definition Multimedia Interface (HDMI) and DisplayPort (DP) Interfaces

Standard	Notes
High-Definition Multimedia Interface (HDMI) Specification, version 2.0a/b	> 340MHz pixel clock Scrambling support Clock/4 support (1/40 bit-rate clock)
VESA DisplayPort Standard Version 1.2a	

A standard DP 1.2a or HDMI 2.0 interface is supported. These share the same set of interface pins, so either DisplayPort or HDMI can be supported natively. Dual-Mode DisplayPort (DP++) can be supported, in which the DisplayPort connector logically outputs TMDS signaling to a DP-to-HDMI dongle.

NOTE: A single CEC controller is shared between HDMI and DP interfaces and can only be applied for use on one interface (i.e., does not support multiple instances if both interfaces were used for HDMI).

Features:

- HDMI
  - HDMI 2.0 mode (3.4Gbps < data rate <= 6Gbps)
  - HDMI 1.4 mode (data rate<=3.4Gbps)
  - Multi-channel audio from HDA controller, up to 8 channels 192kHz 24-bit.
  - Vendor Specific Info-frame (VSI) packet transmission
  - 24-bit RGB and 24-bit YUV444 (HDMI) pixel formats
  - Transition Minimized Differential Signaling (TMDS) functional up to 340MHz pixel clock rate

Table 37 HDMI Signal Descriptions

Signal Name	Type	Description
DP[1:0]_TX3+/-	O	HDMI Differential Clock.
DP[1:0]_TX[2:0]+/-	O	HDMI/DP Differential Data. See the *Jetson TX2/TX2i OEM Product Design Guide* for pin mapping, connection examples and AC coupling requirements on carrier board.
DP[1:0]_HPD	I	Hot plug detection.
HDMI_CEC	I/O	Consumer Electronics Control (CEC) one-wire serial bus. NVIDIA provides low level CEC APIs (read/write). These are not supported in earlier Android releases. For additional CEC support, 3rd party libraries need to be made available.
DP[1:0]_AUX_CH+/-	I/O	HDMI DDC interface.
HDMI 5V Supply	P	HDMI 5V supply to connector:

Table 38 DP Signal Descriptions

Signal Name	Type	Description
DP[1:0]_TX[3:0]+/-	O	DP Differential Lanes.
DP[1:0]_HPD	I	Hot plug detection.
DP[1:0]_AUX_CH+/-	I/O	DP auxiliary channel.
HDMI_CEC	I/O	Consumer Electronics Control (CEC) one-wire serial bus. NVIDIA provides low level CEC APIs (read/write). These are not supported in earlier Android releases. For additional CEC support, 3rd party libraries need to be made available.

4.4.3 Embedded DisplayPort (eDP) Interface

Standard	Notes
VESA Embedded DisplayPort Standard Version 1.4	Supported eDP 1.4 features: ▪ Additional link rates ▪ Enhanced framing ▪ Power sequencing ▪ Reduced aux timing ▪ Reduced main voltage swing

eDP is a mixed-signal interface consisting of 4 differential serial output lanes and 1 PLL. This PLL is used to generate a high frequency bit-clock from an input pixel clock enabling the ability to handle 10-bit parallel data per lane at the pixel rate for the desired mode. Embedded DisplayPort (eDP) modes (1.6GHz for RBR, 2.16GHz, 2.43GHz, 2.7GHz for HBR, 3.42GHz, 4.32GHz and 5.4GHz for HBR2).

NOTE: eDP has been tested according to DP1.2b PHY CTS even though eDPv1.4 supports lower swing voltages and additional intermediate bit rates. This means the following nominal voltage levels (400mV, 600mV, 800mV, 1200mV) and data rates (RBR, HBR, HBR2) are tested. This interface can be tuned to drive lower voltage swings below 400mV and can be programmed to other intermediate bit rates as per the requirements of the panel and the system designer.

The eDP block collects pixels from the output of the display pipeline, formats/encodes them to the eDP format, and then streams them to various output devices. It drives local panels only (does not support an external DP port), includes a small test pattern generator and CRC generator.

Features:

- eDP 1.4
  - 1/2/4 lanes, single link
  - RBR/HBR/HBR2
  - 18/24/36-bit color depth
  - Up to 540 MHz
  - Internal panel: 4096 x 2160 @ 60Hz (2D – portrait/landscape); 1920 x 1080 @ 60Hz (3D – portrait/landscape)
  - -0.5% down spread support
- Stereo mode
- Generic info-frame
- Supports DP AUX and HPD
- Single PHY to output eDP
  - 4-lane eDP
  - Supports 5.4 GHz eDP

Table 39 eDP Signal Descriptions

Signal Name	Type	Description
DP[1:0]_TX[3:0]+ DP[1:0]_TX[3:0]–	Output	eDP Differential lanes
DP[1:0]_HPD	Input	eDP hot-plug detect
DP[1:0]_AUX_CH+ DP[1:0]_AUX_CH–	Bidirectional	eDP Auxiliary channel

4.5 Audio Controllers and Interfaces

4.5.1 Inter-IC Sound (I2S) Controller

The Inter-IC Sound (I2S) controller implements full-duplex, bidirectional and single direction point-to-point serial interfaces. It can interface with I2S-compatible products, such as compact disc players, digital audio tape devices, digital sound processors, modems, Bluetooth chips, etc. The Jetson TX2 series module supports four I2S audio outputs with I2S/PCM interfaces supporting clock rates up to 49.152MHz.

Features:

- Basic I2S modes supported (I2S, RJM, LJM and DSP) in both Master and Slave modes.
- PCM mode with short (one-bit-clock wide) and long-fsync (two bit-clocks wide) in both master and slave modes.
- Network (Telephony) mode with independent slot-selection for both Tx and Rx
- TDM mode with flexibility in number of slots and slot(s) selection.
- Capability to drive-out a High-z outside the prescribed slot for transmission
- Flow control for the external input/output stream.

Table 40 I2S Signal Descriptions

Signal Name	Type	Description
I2S[3:0]_LRCK	I/O	Frame Sync/Word Select. Supports I2S/PCM audio. Interface can be master or slave
I2S[3:0]_SCLK	I/O	Serial Clock/Bit Clock. Supports I2S/PCM audio. Interface can be master or slave
I2S[3:0]_SDIN	I	Data In. Supports I2S/PCM audio. Interface can be master or slave.
I2S[3:0]_SDOUT	I/O	Data Out. Supports I2S/PCM audio. Interface can be master or slave.
AUD_MCLK	O	Audio Codec Master Clock: Connect to clock pin of Audio Codec.
GPIO19_AUD_RST	O	Audio Reset: Connect to reset pin of Audio Codec.
GPIO20_AUD_INT	I	Audio Interrupt: Connect to interrupt pin of Audio Codec.

Table 41. TDM Timing Parameters (Master Mode)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{SCK}	Frequency			24.576	Mhz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$			ns	
T_{FDLY}	I2Sx_LRCK delay	0		4.5	ns	
t_{DDLY}	I2Sx_SDOUT delay	0		4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	-	-	ns	
t_{DH}	I2Sx_SDIN hold time	2	-	-	ns	
t_{RT}	I2Sx_SCLK rise time			5% * T_{CYL}		
t_{FT}	I2Sx_SCLK fall time			5% * T_{CYL}		
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}				
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}				

Table 42. TDM Timing Parameters (Slave Mode up to 24.576Mhz)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{SCK}	Frequency			24.576	Mhz	
T_{CYL}	I2Sx_SCLK cycle time	$1/F_{SCK}$			ns	
t_{DDLY}	I2Sx_SDOUT delay	0		4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	–	ns	
t_{DH}	I2Sx_SDIN hold time	2			ns	
t_{FSU}	I2Sx_LRCK setup	2		45% * T_{CYL} - 2	ns	1
t_{FSH}	I2Sx_LRCK hold	55% T_{CYL} + 2			ns	2
t_{RT}	I2Sx_SCLK rise time			5% * T_{CYL}		
t_{FT}	I2Sx_SCLK fall time			5% * T_{CYL}		
t_{CH}	I2Sx_SCLK high time	45% * T_{CYL}				
t_{CL}	I2Sx_SCLK low time	45% * T_{CYL}				

1. Max t_{FSU} requirement only applies while Fsync Launching on Clock Raising Edge
2. Min t_{FSH} (55% T_{CYL} + 2) requirement only applies while Fsync Launching on Clock Raising Edge; in other use cases, Min t_{FSH} is 2ns.

Table 43. TDM Timing Parameters (Slave Mode up to 12.288Mhz)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{SCK}	Frequency			12.288	Mhz	
T_{CYL}	I2Sx_SCLK cycle time	1/Fsck			ns	
t_{DDLY}	I2Sx_SDOUT delay	0		4.5	ns	
t_{DSU}	I2Sx_SDIN setup time	2	–	–	ns	
t_{DH}	I2Sx_SDIN hold time	2			ns	
t_{FSU}	I2Sx_LRCK setup	2		35% * TCYL - 2	ns	1
t_{FSH}	I2Sx_LRCK hold	65% TCYL + 2			ns	2
t_{RT}	I2Sx_SCLK rise time			15%* TCYL		
t_{FT}	I2Sx_SCLK fall time			15%* TCYL		
t_{CH}	I2Sx_SCLK high time	35% * TCYL				
t_{CL}	I2Sx_SCLK low time	35% * TCYL				

1. Max t_{FSU} requirement only applies while Fsync Launching on Clock Raising Edge
2. Min t_{FSH} (35% T_{CYL} + 2) requirement only applies while Fsync Launching on Clock Raising Edge; in other use cases, Min t_{FSH} is 2ns.

4.5.2 Digital MIC Controller (DMIC)

The DMIC Controller is used to interface with PDM base input devices. The DMIC controller converts Pulse Density Modulation (PDM) signals to Pulse Code Modulation (PCM) signals.

Features:

- Sample rate support: 8 kHz - 48 kHz
- Input PCM bit width: 16 - 24 bits
- Oversampling Ratio: 64, 128, 256

Table 44 DMIC Signal Descriptions

Signal Name	Type	Description
AO_DMIC_IN_CLK	O	Digital MIC Input Clock
AO_DMIC_IN_DAT	I	Digital MIC Input Data

4.5.3 Digital Speaker Controller (DSPK)

The PDM transmit block converts multi-bit PCM audio input to oversampled 1-bit PDM output. The mono or stereo audio is transmitted over a data/clock pair (I2S interface) to an external codec. The block consists of an interpolator followed by a delta sigma modulator (DSM).

- Sample rate support: 8 – 48 kHz
- Input PCM bit-width: 16 – 24 bits
- Oversampling Ratio: 64, 128, 256
- Passband frequency response: <= 0.5 dB peak-to-peak in 10 Hz – 20 kHz range
- THD+N: <= -80 dB @ -10 dBFS
- Dynamic Range: >= 105 dB

Table 45 DSPK Signal Descriptions

Signal Name	Type	Description
DSPK_OUT_CLK	O	Digital Speaker Output Clock
DSPK_OUT_DAT	O	Digital Speaker Ouput Data

4.6 Serial Peripheral Interface

The SPI controllers operate up to 65 Mbps in master mode and 45 Mbps in slave mode. It allows a duplex, synchronous, serial communication between the controller and external peripheral devices. It consists of 4 signals, SS_N (Chip select), SCK (clock), MOSI (Master data out and Slave data in) and MISO (Slave data out and master data in). The data is transferred on MOSI or MISO based on the data transfer direction on every SCK edge. The receiver always receives the data on the other edge of SCK.

Features:

- Independent RX FIFO and TX FIFO.
- Software controlled bit-length supports packet sizes of 1 to 32 bits.
- Packed mode support for bit-length of 7 (8-bit packet size) and 15 (16-bit packet size).
- SS_N can be selected to be controlled by software, or it can be generated automatically by the hardware on packet boundaries.
- Receive compare mode (controller listens for a specified pattern on the incoming data before receiving the data in the FIFO).
- Simultaneous receive and transmit supported

Table 46 SPI Signal Descriptions

Signal Name	Type	Description
SPI2_CS[1:0]# SPI1_CS0# SPI0_CS0#	Bidirectional	Chip Select options for SPI[2:0]: Depending on pin multiplexing, there may be one or more chip select options for each SPI interface. Multiple available chip selects can be used to differentiate between two or more SPI slave devices
SPI[2:0]_MISO	Bidirectional	Master In / Slave Out.
SPI[2:0]_MOSI	Bidirectional	Master Out / Slave In.
SPI[2:0]_CLK	Bidirectional	Serial Clock: Clock phase and polarity are programmable.

Figure 5 SPI Master Timing Diagram

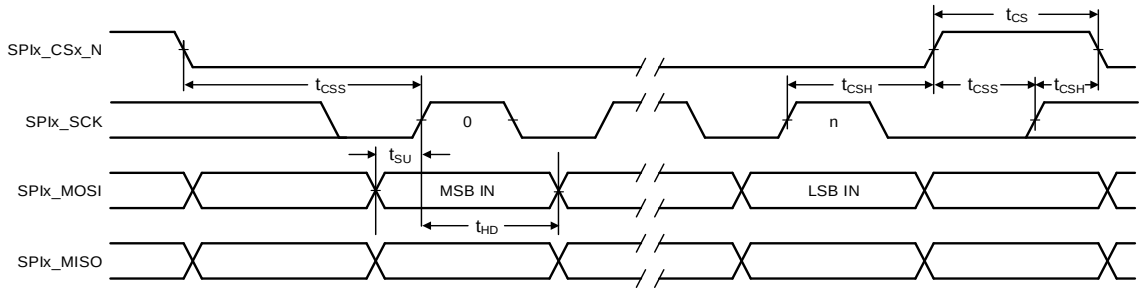


Table 47 SPI Master Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
Fsck	SPIx_SCK clock frequency			65	MHz
Psck	SPIx_SCK period	1/Fsck			ns
t_{CH}	SPIx_SCK high time	50%Psck -10%		50%Psck +10%	ns
t_{CL}	SPIx_SCK low time	50%Psck -10%		50%Psck +10%	ns
t_{CRT}	SPIx_SCK rise time (slew rate)	0.1			V/ns
t_{CFT}	SPIx_SCK fall time (slew rate)	0.1			V/ns
t_{SU}	SPIx_MOSI setup to SPIx_SCK rising edge	2			ns
t_{HD}	SPIx_MOSI hold from SPIx_SCK rising edge	3			ns
t_{CSS}	SPIx_CSx_N setup time	2			ns
t_{CSH}	SPIx_CSx_N hold time	3			ns
t_{CS}	SPIx_CSx_N high time	10			ns

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

Figure 6 SPI Slave Timing Diagram

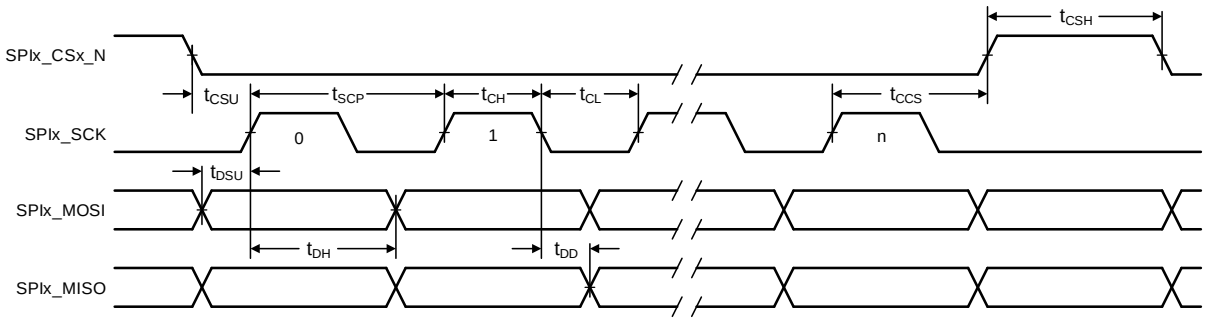


Table 48 SPI Slave Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCP}	SPIx_SCK period	$2*(t_{SDD}+ t_{MSU}$[1]$)$			ns
t_{SCH}	SPIx_SCK high time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCL}	SPIx_SCK low time	$t_{SDD} + t_{MSU}$[1]			ns
t_{SCSU}	SPIx_CSx_n setup time	1			t_{SCP}
t_{SCSH}	SPIx_CSx_n high time	1			t_{SCP}
t_{SCCS}	SPIx_SCK rising edge to SPIx_CSx_n rising edge	1		1	t_{SCP}
t_{SDSU}	SPIx_MOSI setup to SPIx_SCK rising edge	1		1	ns
t_{SDH}	SPIx_MOSI hold from SPIx_SCK rising edge	2		11	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT1[2])	3.5		16	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT2[2])	3		13	ns
t_{SDD}	SPIx_MISO delay from SPIx_SCLK falling edge (ALT3[2])	4		17	ns

1. t_{MSU} is the setup time required by the external master
2. ALT1/2/3 refers to the position of the SPI pins in the Signal Pinout Multiplexing tables in Section 3.1, *Signal List and Multiplexing Functions*.

Note: Polarity of SCLK is programmable. Data can be driven or input relative to either the rising edge (shown above) or falling edge.

4.7 Inter-Chip Communication (I2C) Controller

Standard	Notes
NXP inter-IC-bus (I^2C) specification; Rev 03 — June 2007	Does NOT support: ▪ Multi-master operation ▪ High-speed mode (up to 3.4Mbit/s) ▪ 10-bit slave address

This general purpose I2C controller allows system expansion for I2C-based devices, such as AM/FM radio, remote LCD display, serial ADC/DAC, and serial EPROMs, as defined in the NXP inter-IC-bus (I^2C) specification. The I2C bus supports serial device communications to multiple devices; the I2C controller handles clock source negotiation, speed negotiation for standard and fast devices, 7-bit slave address support according to the I2C protocol and supports master and slave mode of operation.

The I2C controller supports the following operating modes: Master – Standard-mode (up to 100Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1Mbit/s); Slave – Standard-mode (up to 100Kbit/s), Fast-mode (up to 400 Kbit/s), Fast-mode plus (Fm+, up to 1Mbit/s).

Table 49 I2C Usage

Interface (Balls) name	Target Application	On-Module Termination
I2C_GP[3,2,0]_CLK/DAT	General: connect to CLK/Data pins of 1.8V devices	1kΩ pull-ups to VDD_1V8
I2C_GP1_CLK/DAT	General: connect to CLK/Data pins of 3.3V devices	1kΩ pull-ups to VDD_3V3_SYS
I2C_PM_CLK/DAT	Power monitor: connect to CLK/Data pins of 1.8V devices	1kΩ pull-ups to VDD_1V8
I2C_CAM_CLK/DAT	Camera & Camera related functions: Connect to CLK/Data pins of any 1.8V devices	1kΩ pull-ups to VDD_1V8
DP[1:0]_AUX_CH+/-	DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock & Data (HDMI)	See eDP/HDMI/DP sections in the *Jetson TX2/TX2i OEM Product Design Guide* for correct termination. Alternate use: 1.8V/3.3V miscellaneous I2C

Table 50 I2C Signal Descriptions

Signal Name	Type	Description
I2C_GP[3:0]_CLK I2C_PM_CLK I2C_CAM_CLK	Bidirectional	Serial Clock for I2C interfaces.
I2C_GP[3:0]_DAT I2C_PM_DAT I2C_CAM_DAT	Bidirectional	Serial Data for I2C interfaces.

4.8 UART Controller

UART controller provides serial data synchronization and data conversion (parallel-to-serial and serial-to-parallel) for both receiver and transmitter sections. Synchronization for serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character. Data integrity is accomplished by attaching a parity bit to the data character. The parity bit can be checked by the receiver for any transmission bit errors.

NOTE: The UART receiver input has low baud rate tolerance in 1-stop bit mode. External devices must use 2 stop bits. In 1-stop bit mode, the Tegra UART receiver can lose sync between Tegra receiver and the external transmitter resulting in data errors/corruption. In 2-stop bit mode, the extra stop bit allows the Tegra UART receiver logic to align properly with the UART transmitter.

Features:

- Synchronization for the serial data stream with start and stop bits to transmit data and form a data character
- Supports both 16450- and 16550-compatible modes. Default mode is 16450
- Device clock up to 200MHz, baud rate of 12.5Mbits/second
- Data integrity by attaching parity bit to the data character
- Support for word lengths from five to eight bits, an optional parity bit and one or two stop bits
- Support for modem control inputs
- DMA capability for both TX and RX
- 8-bit x 36 deep TX FIFO
- 11-bit x 36 deep RX FIFO. 3 bits of 11 bits per entry will log the RX errors in FIFO mode (break, framing and parity errors as bits 10,9,8 of FIFO entry)
- Auto sense baud detection
- Timeout interrupts to indicate if the incoming stream stopped
- Priority interrupts mechanism
- Flow control support on RTS and CTS
- Internal loopback
- SIR encoding/decoding (3/16 or 4/16 baud pulse widths to transmit bit zero)

Table 51 UART Signal Descriptions

Function	Type	Description
UART[7,3:0]_TX	Output	UART Transmit
UART[7,3:0]_RX	Input	UART Receive
UART[3:0]_CTS#	Input	UART Clear-to-send
UART[3:0]_RTS#	Output	UART Request-to-send

4.9 Video Input Interfaces

NVCSI is the host for the fourth-generation camera solution (NVCSI 1.0, VI 4.0, and ISP 4.0). It is based on the MIPI CSI-2 v1.3 protocol stack; supports D-PHY v1.2; and is paired with the 4th generation NVIDIA video input (VI) unit. The NVCSI combination host enables three 4-lane, six 2-lane, or six 1-lane configurations. Each lane can support up to four virtual channels and supports data type interleaving.

Features:

- Virtual Channel Interleaving
- Data Type Interleaving
- Parallel pixel processing for higher throughput and lower clock speeds

4.9.1 MIPI Camera Serial Interface (CSI)

Standard	Notes
MIPI CSI 2.0 Receiver specification	
MIPI D-PHY® v1.2 Physical Layer specification	

The Jetson TX2 series module supports three MIPI CSI x4 bricks allowing for a variety of device types and camera configurations. Data aggregated from physical lanes enters an asynchronous FIFO which interfaces to the NVCSI block. Each data channel has peak bandwidth of up to 2.5Gbps.

Features:

- Up to three quad lane stereo cameras or 6 dual lane camera streams
- Supported per-brick camera configurations: 1x 4 lanes, 2x 2 lanes, 2x 1 lane, 1x 1 lane, 1x 2 lanes, 1x 1 lane + 1x 2 lanes
- Supports single-shot mode
- Supported input data formats:
  - RGB: RGB888, RGB666, RGB565, RGB555, RGB444
  - YUV: YUV422-8b, YUV420-8b (legacy), YUV420-8b
  - RAW: RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - DPCM (predictor 1): 14-10-14, 14-8-14, 12-8-12, 12-7-12, 12-6-12, 10-8-10, 10-7-10, 10-6-10
  - Embedded control information
- MIPI D-PHY Modes of Operation
  - High Speed Mode – High speed differential signaling up to 2.5Gbps; burst transmission for low power
  - Low Power Control – Single-ended 1.2V CMOS level. Low speed signaling for handshaking.
  - Low Power Escape –Low speed signaling for data, used for escape command entry only. 20Mbps

Table 52 CSI Signal Descriptions

Signal Name	Type	Description
CSI_[5:0]_CLK_N CSI_[5:0]_CLK_P	Input	Differential CSI clock
CSI_[5:0]_D[1:0]_N CSI_[5:0]_D[1:0]_P	Input	Differential CSI data lanes. Each data pair can be associated with a different camera, or CSI_[1:0]_D[1:0], CSI_[3:2]_D[1:0], CSI_[5:4]_D[1:0] can be used to interface with quad-lane cameras.

4.9.2 Camera / VI (Video Input)

The Video Input (VI) block receives data from the CSI receiver and prepares it for presentation to system memory or the dedicated image signal processor (ISP) execution resources. The VI block provides formatting for RGB, YCbCr, and raw Bayer data in support of a number of camera user models. These models include single and multi-camera systems, which may have up to six active streams. The input streams are obtained from MIPI compliant CMOS sensor camera modules.

Table 53 Camera Clock & Control Signal Descriptions

Signal Name	Type	Description
I2C_CAM_CLK	Bidirectional	See I2C section
I2C_CAM_DAT	Bidirectional	See I2C section
CAM[2:0]_MCLK	Output	Video Input Master clocks for primary & secondary cameras
GPIO1_CAM1_PWR# GPIO0_CAM0_PWR#	Bidirectional	Camera Power Control signals: Connect to powerdown pins on camera(s). Available for use as general purpose I/Os.
GPIO4_CAM_STROBE	Output	Camera Strobe Enable: Connect to camera strobe circuit unless strobe control comes from camera module. Available for use as general purpose I/O
GPIO5_CAM_FLASH_EN	Output	Camera Flash Enable: Connect to flash circuit enable. Available for use as general purpose I/O.
GPIO3_CAM1_RST# GPIO2_CAM0_RST#	Output	Camera Resets: Used for camera module resets. If AutoFocus Enable is required, GPIO3_CAM1_RST# to AF_EN pin on camera module & use GPIO2_CAM0_RST# as common reset line. Available for use as general purpose I/Os.
CAM_VSYNC	Output	Camera Vertical Sync

4.10 Controller Area Network (CAN) Interface

Standard	Notes
ISO 11898-1:2006/11898-1:2015 Road vehicles — Controller area network (CAN) Part 1: Data link layer and physical signaling	CAN controller tested with 1-Mbps CAN PHY

The Jetson TX2 series module supports connectivity to two CAN networks.

Features:

- CAN protocol version 2.0A, version 2.0B and ISO 11898-1:2006/11898-1:2015
  - Support ISO11898-1:2006 FD format and BOSCH FD format
  - Dual clock source, enabling FM-PLL designs
  - 16, 32, 64 or 128 Message Objects (configurable)
  - Each Message Object has its own Identifier Mask
  - Programmable FIFO mode
  - Programmable loop-back mode for self-test
- Parity check for Message RAM (optional)
  - Maskable interrupt, two interrupt lines
  - MA support, automatic Message Object increment
  - Power-down support

- Supports TT CAN
  - TTCAN Level 0, 1, and 2
  - Time Mark Interrupts
  - Stop Watch
  - Watchdog Timer
  - Synchronization to external events

Table 54 CAN Signal Descriptions

Signal Name	Type	Description
CAN_WAKE	I	Wake
CAN[1:0]_RX	I	CAN Receive (RX) Bus
CAN[1:0]_TX	O	CAN Transmit (TX) Bus
CAN[1:0]_ERR	I	Error
CAN1_STBY	O	Standby

4.11 JTAG

An optional JTAG interface is available for SCAN testing or can be used for communicating with either integrated CPU.

Table 55 Debug Signal Descriptions

Signal Name	Type	Description
JTAG_RTCK	Output	Return Test Clock
JTAG_TCK	Input	Test Clock
JTAG_TDI	Input	Test Data In
JTAG_TDO	Output	Test Data Out
JTAG_TMS	Input	Test Mode Select
JTAG_GP0	Input	Test Reset
JTAG_GP1	Input	General Purpose. Pulled low on module for normal operation & pulled high by test device for Boundary Scan test mode

5.0 Pin Definitions

The function(s) for each pin on the Jetson TX2 series module is fixed to a single Special-Function I/O (SFIO) or software-controlled General Purpose I/O (GPIO). The Jetson TX2 series module has multiple dedicated GPIOs; each GPIO is individually configurable as Output/Input/Interrupt sources with level/edge controls.

SFIO and GPIO functionality is configured using Multi-purpose I/O (MPIO) pads within the Jetson TX2 series module. To achieve system operation without the need of a lot of additional on-board components, the Jetson TX2 series module utilizes six types of MPIO pads:

- ST (standard) pads are the most common pads on the chip; they are used for typical General Purpose I/O.
- DD (dual-driver) pads are similar to the ST pads. A DD pad can tolerate its I/O pin being pulled up to 3.3V (regardless of supply voltage) as long as the pad's output-driver is set to open-drain mode. There are special power-sequencing considerations when using this functionality.
- CZ (controlled output impedance) pads are optimized for use in applications requiring tightly controlled output impedance. They are similar to ST pads except for changes in the drive strength circuitry and in the weak pull-ups/-downs.
- LV_CZ (low voltage controlled impedance) pads are similar to CZ pads but are optimized for use with a 1.2V supply voltage (and signaling level). They support a 1.8V supply voltage (and signaling level) as a secondary mode.
- DP_AUX pad is used as an auxiliary control channel for the Display Port which requires differential signaling.

Each MPIO pad consists of:

- An output driver with tristate capability, drive strength controls and push-pull mode, open-drain mode, or both
- An input receiver with either schmitt mode, CMOS mode, or both
- A weak pull-up and a weak pull-down

MPIO pads are partitioned into multiple "pad control groups" with controls being configured for the group. During normal operation, these per-pad controls are driven by the pinmux controller registers. During deep sleep, the PMC bypasses and then resets the pinmux controller registers. Software reprograms these registers as necessary after returning from deep sleep.

Refer to the ***Jetson TX2/TX2i OEM Product Design Guide*** for more information on pad behavior associated with different interfaces and the ***Parker Series SoC Technical Reference Manual*** for more information on modifying MPIO pad controls.

5.1 Power-on Reset Behavior

Each MPIO pad has a deterministic power-on reset (PoR) state. The particular reset state for each pad is chosen to minimize the need of additional on-board components; for example, on-chip weak pull-ups are enabled during PoR for pads which are usually used to drive active-low chip selects eliminating the need for additional pull-up resistors.

The following list is a simplified description of the Jetson TX2 series module boot process focusing on those aspects which relate to the MPIO pins.

1. System-level hardware executes the power-up sequence. This sequence ends when system-level hardware releases SYS_RESET_N.
2. The boot ROM begins executing and programs the on-chip I/O controllers to access the secondary boot device.
3. The boot ROM fetches the Boot Configuration Table (BCT) and boot loader from the secondary boot device.
4. If the BCT and boot loader are fetched successfully, the boot ROM transfers control to the boot loader.
5. Otherwise, the boot ROM enters USB recovery mode.

5.2 Deep Sleep Behavior

Deep Sleep is an ultra-low-power standby state in which the Jetson TX2 series module maintains much of its I/O state while most of the chip is powered off. During deep sleep most of the pads are put in a state called Deep Power Down (DPD). The sequence for entering DPD is same across pads.

ALL MPIO pads **do NOT** have identical behavior during deep sleep. They differ with regard to:

- Input buffer behavior during deep sleep
  - Forcibly disabled OR
  - Enabled for use as a “GPIO wake event” OR
  - Enabled for some other purpose (e.g., a “clock request” pin)
- Output buffer behavior during deep sleep
  - Maintain a static programmable (0, 1, or tristate) constant value OR
  - Capable of changing state (i.e., dynamic while the chip is still in deep sleep)
- Weak pull-up/pull-down behavior during deep sleep
  - Forcibly disabled OR
  - Can be configured
- Pads that do not enter deep sleep
  - Some of the pads whose outputs are dynamic during deep sleep are of special type and they do not enter deep sleep (e.g., pads that are associated with PMC logic do not enter deep sleep, pads that are associated with JTAG do not enter into deep sleep any time.

5.3 Module Connector Pinout

Table 56 Jetson TX2/TX2i Connector (8x50) Pinout Matrix

Legend:	Ground	Power	Not Available on Jetson TX1	Reserved	Unassigned on Carrier	TX2 / TX2i	Redefined

Notes: RSVD (Reserved) pins on the Jetson TX2/TX2i must be left unconnected. The Orange shaded cells show changes in pinout between TX2 and TX2i

Signals starting with "GPIO_" are standard GPIOs that have been assigned recommended usages. If the assigned usage is required in a design it is recommended the matching GPIO be used. If the assigned usage is not required, the pins may be used as GPIOs for other purposes.

	A	B	C	D	E	F	G	H	
1	VDD_IN	VDD_IN	VDD_IN	RSVD	FORCE_RECOV#	AUDIO_MCLK	I2S0_SDIN	I2S0_LRCLK	1
2	VDD_IN	VDD_IN	VDD_IN	RSVD	SLEEP#	GPIO19_AUD_RST	I2S0_CLK	I2S0_SDOUT	2
3	GND	GND	GND	RSVD	SPI0_CLK	SPI0_CS0#	GND	GPIO20_AUD_INT	3
4	GND	GND	GND	RSVD	SPI0_MISO	SPI0_MOSI	DSPK_OUT_CLK	DSPK_OUT_DAT	4
5	RSVD	RSVD	RSVD	UART7_RX	I2S3_SDIN	I2S3_LRCLK	I2S2_CLK	I2S2_LRCLK	5
6	I2C_PM_CLK	I2C_PM_DAT	I2C_CAM_CLK	I2C_CAM_DAT	I2S3_CLK	I2S3_SDOUT	I2S2_SDIN	I2S2_SDOUT	6
7	CHARGING#	CARRIER_STBY#	BATLOW#	GPIO5_CAM_FLASH_EN	CAM2_MCLK	GPIO1_CAM1_PWR#	GPIO4_CAM_STROBE	GPIO3_CAM1_RST#	7
8	GPIO14_AP_WAKE_MDM	VIN_PWR_BAD#	BATT_OC	UART7_TX	CAM_VSYNC	CAM1_MCLK	GPIO0_CAM0_PWR#	GPIO2_CAM0_RST#	8
9	GPIO15_AP2MDM_READY	GPIO17_MDM2AP_READY	WDT_TIME_OUT#	UART1_TX	UART1_RTS#	CAM0_MCLK	UART3_CTS#	UART3_RX	9
10	GPIO16_MDM_WAKE_AP	GPIO18_MDM_COLDBOOT	I2C_GP2_DAT	UART1_RX	UART1_CTS#	GND	UART3_RTS#	UART3_TX	10
11	JTAG_GP1	JTAG_TCK	I2C_GP2_CLK	RSVD	RSVD	RSVD	UART0_RTS#	UART0_CTS#	11
12	JTAG_TMS	JTAG_TDI	I2C_GP3_CLK	RSVD	RSVD	RSVD	UART0_RX	UART0_TX	12
13	JTAG_TDO	JTAG_GP0	I2C_GP3_DAT	I2S1_LRCLK	RSVD	SPI1_MOSI	SPI1_CLK	GPIO8_ALS_PROX_INT	13
14	JTAG_RTCK	GND	I2S1_SDIN	I2S1_SDOUT	SPI1_CS0#	SPI1_MISO	GPIO9_MOTION_INT	SPI2_CLK	14
15	UART2_CTS#	UART2_RX	I2S1_CLK	I2C_GP0_DAT	I2C_GP0_CLK	GND	SPI2_MOSI	SPI2_MISO	15
16	UART2_RTS#	UART2_TX	FAN_PWM	AO_DMIC_IN_DAT	AO_DMIC_IN_CLK	SPI2_CS1#	SPI2_CS0#	SDCARD_PWR_EN	16
17	USB0_EN_OC#	FAN_TACH	CAN1_STBY	CAN1_RX	RSVD	SDCARD_CD#	GND	SDCARD_D1	17
18	USB1_EN_OC#	RSVD	CAN1_TX	CAN0_RX	CAN0_ERR	SDCARD_D3	SDCARD_CLK	SDCARD_D0	18
19	RSVD	GPIO11_AP_WAKE_BT	CAN1_ERR	CAN0_TX	GND	SDCARD_D2	SDCARD_CMD	GND	19
20	I2C_GP1_DAT	GPIO10_WIFI_WAKE_AP	CAN_WAKE	GND	CSI5_D1-	SDCARD_WP	GND	CSI4_D1-	20
21	I2C_GP1_CLK	GPIO12_BT_EN	GND	CSI5_CLK-	CSI5_D1+	GND	CSI4_CLK-	CSI4_D1+	21
22	GPIO_EXP1_INT	GPIO13_BT_WAKE_AP	CSI5_D0-	CSI5_CLK+	GND	CSI4_D0-	CSI4_CLK+	GND	22
23	GPIO_EXP0_INT	GPIO7_TOUCH_RST	CSI5_D0+	GND	CSI3_D1-	CSI4_D0+	GND	CSI2_D1-	23
24	LCD1_BKLT_PWM	TOUCH_CLK	GND	CSI3_CLK-	CSI3_D1+	GND	CSI2_CLK-	CSI2_D1+	24
25	LCD_TE	GPIO6_TOUCH_INT	CSI3_D0-	CSI3_CLK+	GND	CSI2_D0-	CSI2_CLK+	GND	25
26	GSYNC_HSYNC	LCD_VDD_EN	CSI3_D0+	GND	CSI1_D1-	CSI2_D0+	GND	CSI0_D1-	26
27	GSYNC_VSYNC	LCD0_BKLT_PWM	GND	CSI1_CLK-	CSI1_D1+	GND	CSI0_CLK-	CSI0_D1+	27
28	GND	LCD_BKLT_EN	CSI1_D0-	CSI1_CLK+	GND	CSI0_D0-	CSI0_CLK+	GND	28
29	SDIO_RST#	RSVD / SDIO_CMD	CSI1_D0+	GND	DSI3_D1+	CSI0_D0+	GND	DSI2_D1+	29
30	RSVD / SDIO_D3	RSVD / SDIO_CLK	GND	DSI3_CLK+	DSI3_D1-	GND	DSI2_CLK+	DSI2_D1-	30
31	RSVD / SDIO_D2	GND	DSI3_D0+	DSI3_CLK–	GND	DSI2_D0+	DSI2_CLK-	GND	31
32	RSVD / SDIO_D1	RSVD / SDIO_D0	DSI3_D0-	GND	DSI1_D1+	DSI2_D0-	GND	DSI0_D1+	32
33	DP1_HPD	HDMI_CEC	GND	DSI1_CLK+	DSI1_D1-	GND	DSI0_CLK+	DSI0_D1-	33
34	DP1_AUX_CH-	DP0_AUX_CH-	DSI1_D0+	DSI1_CLK–	GND	DSI0_D0+	DSI0_CLK-	GND	34
35	DP1_AUX_CH+	DP0_AUX_CH+	DSI1_D0-	GND	DP1_TX3-	DSI0_D0-	GND	DP0_TX3-	35
36	USB0_OTG_ID	DP0_HPD	GND	DP1_TX2-	DP1_TX3+	GND	DP0_TX2-	DP0_TX3+	36
37	GND	USB0_VBUS_DET	DP1_TX1-	DP1_TX2+	GND	DP0_TX1-	DP0_TX2+	GND	37
38	USB1_D+	GND	DP1_TX1+	GND	DP1_TX0-	DP0_TX1+	GND	DP0_TX0-	38
39	USB1_D-	USB0_D+	GND	PEX_RFU_TX+	DP1_TX0+	GND	PEX_RFU_RX+	DP0_TX0+	39
40	GND	USB0_D-	PEX2_TX+	PEX_RFU_TX-	GND	PEX2_RX+	PEX_RFU_RX-	GND	40
41	PEX2_REFCLK+	GND	PEX2_TX-	GND	PEX1_TX+	PEX2_RX-	GND	PEX1_RX+	41
42	PEX2_REFCLK–	USB2_D+	GND	USB_SS1_TX+	PEX1_TX-	GND	USB_SS1_RX+	PEX1_RX-	42
43	GND	USB2_D-	USB_SS0_TX+	USB_SS1_TX-	GND	USB_SS0_RX+	USB_SS1_RX-	GND	43
44	PEX0_REFCLK+	GND	USB_SS0_TX-	GND	PEX0_TX+	USB_SS0_RX-	GND	PEX0_RX+	44
45	PEX0_REFCLK-	PEX1_REFCLK+	GND	SATA_TX+	PEX0_TX-	GND	SATA_RX+	PEX0_RX-	45
46	RESET_OUT#	PEX1_REFCLK-	PEX2_CLKREQ#	SATA_TX-	GND	GBE_LINK1000#	SATA_RX-	GND	46
47	RESET_IN#	GND	PEX1_CLKREQ#	SATA_DEV_SLP	GBE_LINK_ACT#	GBE_MDI1+	GND	GBE_MDI3+	47
48	CARRIER_PWR_ON	SYS_WAKE#	PEX0_CLKREQ#	PEX_WAKE#	GBE_MDI0+	GBE_MDI1-	GBE_MDI2+	GBE_MDI3-	48
49	CHARGER_PRSNT#	MOD_PWR_CFG_ID	PEX0_RST#	PEX2_RST#	GBE_MDI0-	GND	GBE_MDI2-	GND	49
50	VDD_RTC	POWER_BTN#	RSVD	RSVD	PEX1_RST#	GBE_LINK100#	GND	RSVD	50
	A	B	C	D	E	F	G	H	

5.4 Pin Descriptions

Legend:	Ground	Power	Not Available on Jetson TX1	Reserved on Jetson TX2	Unassigned on Carrier	TX2 / TX2i	Redefined

Table 57 Pin List

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
A1	VDD_IN	Main power – Supplies PMIC & external supplies	Input	5.5V-19.0V (TX2) 9.0V-19.0V (TX2i)	
A2	VDD_IN	Main power – Supplies PMIC & external supplies	Input	5.5V-19.0V (TX2) 9.0V-19.0V (TX2i)	
A3	GND	GND	–	GND	
A4	GND	GND	–	GND	
A5	RSVD	Not used	–	–	
A6	I2C_PM_CLK	PM I2C Bus Clock	Bidir	Open Drain – 1.8V	DD
A7	CHARGING#	Charger Interrupt	Input	CMOS – 1.8V	ST
A8	GPIO14_AP_WAKE_MDM	AP (Tegra) Wake Modem or GPIO	Output	CMOS – 1.8V	LV_CZ
A9	GPIO15_AP2MDM_READY	AP (Tegra) to Modem Ready or GPIO	Output	CMOS – 1.8V	LV_CZ
A10	GPIO16_MDM_WAKE_AP	Modem Wake AP (Tegra) or GPIO	Input	CMOS – 1.8V	ST
A11	JTAG_GP1	JTAG General Purpose	Input	CMOS – 1.8V	
A12	JTAG_TMS	JTAG Test Mode Select	Input	CMOS – 1.8V	
A13	JTAG_TDO	JTAG Test Data Out	Output	CMOS – 1.8V	ST
A14	JTAG_RTCK	JTAG Return Clock	Input	CMOS – 1.8V	
A15	UART2_CTS#	UART 2 Clear to Send	Input	CMOS – 1.8V	ST
A16	UART2_RTS#	UART 2 Request to Send	Output	CMOS – 1.8V	ST
A17	USB0_EN_OC#	USB VBUS Enable	Bidir	Open Drain – 3.3V	DD
A18	USB1_EN_OC#	USB VBUS Enable	Bidir	Open Drain – 3.3V	DD
A19	RSVD	Not used	–	–	
A20	I2C_GP1_DAT	General I2C Bus #1 Data	Bidir	Open Drain – 3.3V	DD
A21	I2C_GP1_CLK	General I2C Bus #1 Clock	Bidir	Open Drain – 3.3V	DD
A22	GPIO_EXP1_INT	GPIO Expander 1 Interrupt or GPIO	Input	CMOS – 1.8V	ST
A23	GPIO_EXP0_INT	GPIO expander 0 Interrupt or GPIO	Input	CMOS – 1.8V	ST
A24	LCD1_BKLT_PWM	Display Backlight PWM #1	Output	CMOS – 1.8V	ST
A25	LCD_TE	Display Tearing Effect	Input	CMOS – 1.8V	ST
A26	GSYNC_HSYNC	GSYNC Horizontal Sync	Output	CMOS – 1.8V	ST
A27	GSYNC_VSYNC	GSYNC Vertical Sync	Output	CMOS – 1.8V	ST
A28	GND	GND	–	GND	
A29	SDIO_RST#	Secondary Wi-Fi Enable	Output	CMOS – 1.8V	ST
A30	RSVD (TX2) / SDIO_D3 (TX2i)	Not used / SDIO Data 3	– / Bidir	– / CMOS – 1.8V	

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
A31	RSVD (TX2) / SDIO_D2 (TX2i)	Not used / SDIO Data 2	– / Bidir	– / CMOS – 1.8V	
A32	RSVD (TX2) / SDIO_D1 (TX2i)	Not used / SDIO Data 1	– / Bidir	– / CMOS – 1.8V	
A33	DP1_HPD	Display Port 1 Hot Plug Detect	Input	CMOS – 1.8V	ST
A34	DP1_AUX_CH–	Display Port 1 Aux– or HDMI DDC SDA	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	
A35	DP1_AUX_CH+	Display Port 1 Aux+ or HDMI DDC SCL	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	
A36	USB0_OTG_ID	USB ID	Input	Analog	
A37	GND	GND	–	GND	
A38	USB1_D+	USB 2.0, Port 1 Data+	Bidir	USB PHY	
A39	USB1_D–	USB 2.0, Port 1 Data–	Bidir	USB PHY	
A40	GND	GND	–	GND	
A41	PEX2_REFCLK+	PCIe Reference Clock 2+	Output	PCIe PHY	
A42	PEX2_REFCLK–	PCIe Reference Clock 2–	Output	PCIe PHY	
A43	GND	GND	–	GND	
A44	PEX0_REFCLK+	PCIe Reference Clock 0+	Output	PCIe PHY	
A45	PEX0_REFCLK–	PCIe Reference Clock 0–	Output	PCIe PHY	
A46	RESET_OUT#	Reset from PMIC (through diodes) to Tegra & eMMC reset pins. Driven from carrier board to force reset of Tegra & eMMC (not PMIC).	Bidir	CMOS – 1.8V	
A47	RESET_IN#	System Reset driven from PMIC to carrier board for devices requiring full system reset. Also driven from carrier board to initiate full system reset (i.e. RESET button).	Bidir	Open Drain – 1.8V	
A48	CARRIER_PWR_ON	Carrier Power On. Used as part of the power up sequence. The module asserts this signal when it is safe for the carrier board to power up.	Output	Open-Collector – 3.3V	
A49	CHARGER_PRSNT#	Connected to PMIC ACOK through FET & 4.7kΩ resistor. PMIC ACOK has 100kΩ pull-up internally to MBATT (VDD_5V0_SYS). Can optionally be used to support auto-power-on where the module platform will power-on when the main power source is connected instead of waiting for a power button press.	Input	MBATT level – 5.0V	
A50	VDD_RTC	Back-up Real-Time-Clock rail (connects to Lithium Cell or super capacitor on Carrier Board). PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Bidir	Power In/Power Out	
B1	VDD_IN	Main power – Supplies PMIC & external supplies	Input	5.5V-19.0V (TX2) 9.0V-19.0V (TX2i)	
B2	VDD_IN	Main power – Supplies PMIC & external supplies	Input	5.5V-19.0V (TX2) 9.0V-19.0V (TX2i)	
B3	GND	GND	–	GND	
B4	GND	GND	–	GND	
B5	RSVD	Not used	–	–	
B6	I2C_PM_DAT	PM I2C Bus Data	Bidir	Open Drain – 1.8V	DD

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
B7	CARRIER_STBY#	SOC Power Request. The module drives this signal low when it is in the standby power state.	Output	CMOS – 1.8V	ST
B8	VIN_PWR_BAD#	Carrier board indication to the module that the VDD_IN power is not valid. Carrier board should de-assert this (drive high) only when VDD_IN has reached its required voltage level and is stable. This prevents Tegra from powering up until the VDD_IN power is stable.	Input	CMOS – 5.0V	
B9	GPIO17_MDM2AP_READY	Modem to AP (Tegra) Ready or GPIO	Input	CMOS – 1.8V	CZ
B10	GPIO18_MDM_COLDBOOT	Modem Coldboot or GPIO	Input	CMOS – 1.8V	CZ
B11	JTAG_TCK	JTAG Test Clock	Input	CMOS – 1.8V	
B12	JTAG_TDI	JTAG Test Data In	Input	CMOS – 1.8V	
B13	JTAG_GP0	JTAG Test Reset	Input	CMOS – 1.8V	
B14	GND	GND	–	GND	
B15	UART2_RX	UART 2 Receive	Input	CMOS – 1.8V	ST
B16	UART2_TX	UART 2 Transmit	Output	CMOS – 1.8V	ST
B17	FAN_TACH	Fan Tach	Input	CMOS – 1.8V	ST
B18	RSVD	Not used	–	–	
B19	GPIO11_AP_WAKE_BT	AP (Tegra) Wake Bluetooth or GPIO	Output	CMOS – 1.8V	ST
B20	GPIO10_WIFI_WAKE_AP	Wi-Fi 2 Wake AP (Tegra) or GPIO	Input	CMOS – 1.8V	ST
B21	GPIO12_BT_EN	BT 2 Enable or GPIO	Output	CMOS – 1.8V	ST
B22	GPIO13_BT_WAKE_AP	BT 2 Wake AP (Tegra) or GPIO	Input	CMOS – 1.8V	ST
B23	GPIO7_TOUCH_RST	Touch Reset or GPIO	Output	CMOS – 1.8V	ST
B24	TOUCH_CLK	Touch Clock	Output	CMOS – 1.8V	ST
B25	GPIO6_TOUCH_INT	Touch Interrupt or GPIO	Input	CMOS – 1.8V	ST
B26	LCD_VDD_EN	Display VDD Enable	Output	CMOS – 1.8V	ST
B27	LCD0_BKLT_PWM	Display Backlight PWM #0	Output	CMOS – 1.8V	ST
B28	LCD_BKLT_EN	Display Backlight Enable	Output	CMOS – 1.8V	ST
B29	RSVD (TX2) / SDIO_CMD (TX2i)	Not used / SDIO Command	– / Bidir	– / CMOS – 1.8V	
B30	RSVD (TX2) / SDIO_CLK (TX2i)	Not used / SDIO Clock	– / Output	– / CMOS – 1.8V	
B31	GND	GND	–	GND	
B32	RSVD (TX2) / SDIO_D0 (TX2i)	Not used / SDIO Data 0	– / Bidir	– / CMOS – 1.8V	
B33	HDMI_CEC	HDMI CEC	Bidir	Open Drain – 3.3V	DD
B34	DP0_AUX_CH–	Display Port 0 Aux– or HDMI DDC SDA	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	
B35	DP0_AUX_CH+	Display Port 0 Aux+ or HDMI DDC SCL	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)	
B36	DP0_HPD	Display Port 0 Hot Plug Detect	Input	CMOS – 1.8V	DD

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
B37	USB0_VBUS_DET	VBUS Detect	Input	USB VBUS, 5V	
B38	GND	GND	–	GND	
B39	USB0_D+	USB 2.0, Port 0 Data+	Bidir	USB PHY	
B40	USB0_D–	USB 2.0, Port 0 Data-	Bidir	USB PHY	
B41	GND	GND	–	GND	
B42	USB2_D+	USB 2.0, Port 2 Data+	Bidir	USB PHY	
B43	USB2_D–	USB 2.0, Port 2 Data-	Bidir	USB PHY	
B44	GND	GND	–	GND	
B45	PEX1_REFCLK+	PCIe Reference Clock 1+	Output	PCIe PHY	
B46	PEX1_REFCLK–	PCIe Reference Clock 1–	Output	PCIe PHY	
B47	GND	GND	–	GND	
B48	SYS_WAKE#	Power button & SC7 wake interrupt	Input	CMOS – 1.8V	
B49	MOD_PWR_CFG_ID	Module power configuration identification. Tied to GND on Jetson TX2i. Floating on Jetson TX2. Determines the power-on mechanism used to support both Jetson TX2 & TX2i.	Output	VDD_IN Level	
B50	POWER_BTN#	Power on. Connected to PMIC EN0 which has internal 10KΩ Pull-up to VDD_5V0_SYS. Also connected to Tegra POWER_ON pin through Diode with 100kΩ pull-up to VDD_1V8_AP near Tegra.	Input	CMOS – 5.0V	
C1	VDD_IN	Main power – Supplies PMIC & external supplies	Input	5.5V-19.0V (TX2) 9.0V-19.0V (TX2i)	
C2	VDD_IN	Main power – Supplies PMIC & external supplies	Input	5.5V-19.0V (TX2) 9.0V-19.0V (TX2i)	
C3	GND	GND	–	GND	
C4	GND	GND	–	GND	
C5	RSVD	Not used	–	–	
C6	I2C_CAM_CLK	Camera I2C Clock	Bidir	Open Drain – 1.8V	DD
C7	BATLOW#	GPIO – Low Battery	Input	CMOS – 1.8V	ST
C8	BATT_OC	Thermal/Over-current Warning	Bidir	CMOS – 1.8V	ST
C9	WDT_TIME_OUT#	Watchdog Timeout	Input	CMOS – 1.8V	ST
C10	I2C_GP2_DAT	General I2C Bus #2 Data	Bidir	Open Drain – 1.8V	DD
C11	I2C_GP2_CLK	General I2C Bus #2 Clock	Bidir	Open Drain – 1.8V	DD
C12	I2C_GP3_CLK	General I2C Bus #3 Clock	Bidir	Open Drain – 1.8V	DD
C13	I2C_GP3_DAT	General I2C Bus #3 Data	Bidir	Open Drain – 1.8V	DD
C14	I2S1_SDIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V	CZ
C15	I2S1_CLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V	CZ
C16	FAN_PWM	Fan PWM	Output	CMOS – 1.8V	ST
C17	CAN1_STBY	CAN #1 Standby	Output	CMOS – 3.3V	CZ
C18	CAN1_TX	CAN #1 Transmit	Output	CMOS – 3.3V	CZ

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
C19	CAN1_ERR	CAN #1 Error	Input	CMOS – 3.3V	CZ
C20	CAN_WAKE	CAN Wake	Input	CMOS – 3.3V	CZ
C21	GND	GND	–	GND	
C22	CSI5_D0–	Camera, CSI 5 Data 0–	Input	MIPI D-PHY	
C23	CSI5_D0+	Camera, CSI 5 Data 0+	Input	MIPI D-PHY	
C24	GND	GND	–	GND	
C25	CSI3_D0–	Camera, CSI 3 Data 0–	Input	MIPI D-PHY	
C26	CSI3_D0+	Camera, CSI 3 Data 0+	Input	MIPI D-PHY	
C27	GND	GND	–	GND	
C28	CSI1_D0–	Camera, CSI 1 Data 0–	Input	MIPI D-PHY	
C29	CSI1_D0+	Camera, CSI 1 Data 0+	Input	MIPI D-PHY	
C30	GND	GND	–	GND	
C31	DSI3_D0+	Display, DSI 3 Data 0+	Output	MIPI D-PHY	
C32	DSI3_D0–	Display, DSI 3 Data 0–	Output	MIPI D-PHY	
C33	GND	GND	–	GND	
C34	DSI1_D0+	Display, DSI 1 Data 0+	Output	MIPI D-PHY	
C35	DSI1_D0–	Display, DSI 1 Data 0–	Output	MIPI D-PHY	
C36	GND	GND	–	GND	
C37	DP1_TX1–	DisplayPort 1 Lane 1– / HDMI Lane 1–	Output	AC-Coupled on carrier board	
C38	DP1_TX1+	DisplayPort 1 Lane 1+ / HDMI Lane 1+	Output	AC-Coupled on carrier board	
C39	GND	GND	–	GND	
C40	PEX2_TX+	PCIe #0 Lane 2 or PCIE #1 Lane 0 Transmit+	Output	PCIe PHY, AC-Coupled on carrier board	
C41	PEX2_TX–	PCIe #0 Lane 2 or PCIE #1 Lane 0 Transmit–	Output	PCIe PHY, AC-Coupled on carrier board	
C42	GND	GND	–	GND	
C43	USB_SS0_TX+	USB 3.0 #1 Transmit+ (muxed w/PEX1)	Output	USB SS PHY, AC-Coupled on carrier board	
C44	USB_SS0_TX–	USB 3.0 #1 Transmit– (muxed w/PEX1)	Output	USB SS PHY, AC-Coupled on carrier board	
C45	GND	GND	–	GND	
C46	PEX2_CLKREQ#	PCIE #2 Clock Request	Bidir	Open Drain 3.3V, Pull-up on the module	DD
C47	PEX1_CLKREQ#	PCIE #1 Clock Request (mux option)	Bidir	Open Drain 3.3V, Pull-up on the module	DD
C48	PEX0_CLKREQ#	PCIE #0 Clock Request	Bidir	Open Drain 3.3V, Pull-up on the module	DD
C49	PEX0_RST#	PCIe #0 Reset	Output	Open Drain 3.3V, Pull-up on the module	DD
C50	RSVD	Not used	–	–	
D1	RSVD	Not used	–	–	
D2	RSVD	Not used	–	–	

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
D3	RSVD	Not used	–	–	
D4	RSVD	Not used	–	–	
D5	UART7_RX	UART 7 Receive	Input	CMOS – 1.8V	ST
D6	I2C_CAM_DAT	Camera I2C Data	Bidir	Open Drain – 1.8V	DD
D7	GPIO5_CAM_FLASH_EN	Camera Flash Enable or GPIO	Output	CMOS – 1.8V	ST
D8	UART7_TX	UART 7 Transmit	Output	CMOS – 1.8V	ST
D9	UART1_TX	UART 1 Transmit	Output	CMOS – 1.8V	ST
D10	UART1_RX	UART 1 Receive	Input	CMOS – 1.8V	ST
D11	RSVD	Not used	–	–	
D12	RSVD	Not used	–	–	
D13	I2S1_LRCLK	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V	CZ
D14	I2S1_SDOUT	I2S Audio Port 1 Data Out	Bidir	CMOS – 1.8V	CZ
D15	I2C_GP0_DAT	General I2C Bus #0 Data	Bidir	Open Drain – 1.8V	CZ
D16	AO_DMIC_IN_DAT	Digital Mic Input Data	Input	CMOS – 1.8V	CZ
D17	CAN1_RX	CAN #1 Receive	Input	CMOS 3.3V	CZ
D18	CAN0_RX	CAN #0 Receive	Input	CMOS 3.3V	CZ
D19	CAN0_TX	CAN #0 Transmit	Output	CMOS 3.3V	CZ
D20	GND	GND	–	GND	
D21	CSI5_CLK–	Camera, CSI 5 Clock–	Input	MIPI D-PHY	
D22	CSI5_CLK+	Camera, CSI 5 Clock+	Input	MIPI D-PHY	
D23	GND	GND	–	GND	
D24	CSI3_CLK–	Camera, CSI 3 Clock–	Input	MIPI D-PHY	
D25	CSI3_CLK+	Camera, CSI 3 Clock+	Input	MIPI D-PHY	
D26	GND	GND	–	GND	
D27	CSI1_CLK–	Camera, CSI 1 Clock–	Input	MIPI D-PHY	
D28	CSI1_CLK+	Camera, CSI 1 Clock+	Input	MIPI D-PHY	
D29	GND	GND	–	GND	
D30	DSI3_CLK+	Display DSI 3 Clock+	Output	MIPI D-PHY	
D31	DSI3_CLK–	Display DSI 3 Clock–	Output	MIPI D-PHY	
D32	GND	GND	–	GND	
D33	DSI1_CLK+	Display DSI 1 Clock+	Output	MIPI D-PHY	
D34	DSI1_CLK–	Display DSI 1 Clock–	Output	MIPI D-PHY	
D35	GND	GND	–	GND	
D36	DP1_TX2–	DisplayPort 1 Lane 2– / HDMI Lane 0–	Output	AC-Coupled on carrier board	
D37	DP1_TX2+	DisplayPort 1 Lane 2+ / HDMI Lane 0+	Output	AC-Coupled on carrier board	
D38	GND	GND	–	GND	

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
D39	PEX_RFU_TX+	PCIe RFU Transmit+ (PCIe #0 Lane 3 or USB 3.0 port #1)	Output	PCIe PHY, AC-Coupled on carrier board	
D40	PEX_RFU_TX–	PCIe RFU Transmit- (PCIe #0 Lane 3 or USB 3.0 port #1)	Output	PCIe PHY, AC-Coupled on carrier board	
D41	GND	GND	–	GND	
D42	USB_SS1_TX+	USB SS1 RFU Transmit+ (PCIe #0 Lane 1 or USB 3.0 port #2)	Output	USB SS PHY, AC-Coupled on carrier board	
D43	USB_SS1_TX–	USB SS1 RFU Transmit- (PCIe #0 Lane 1 or USB 3.0 port #2)	Output	USB SS PHY, AC-Coupled on carrier board	
D44	GND	GND	–	GND	
D45	SATA_TX+	SATA Transmit+	Output	SATA PHY, AC-Coupled on carrier board	
D46	SATA_TX–	SATA Transmit–	Output	SATA PHY, AC-Coupled on carrier board	
D47	SATA_DEV_SLP	SATA Device Sleep or PEX1_CLKREQ# depending on Mux setting	Input	Open Drain 3.3V, Pull-up on the module	DD
D48	PEX_WAKE#	PCIe Wake	Input	Open Drain 3.3V, Pull-up on the module	DD
D49	PEX2_RST#	PCIe #2 Reset	Output	Open Drain 3.3V, Pull-up on the module	DD
D50	RSVD	Not used	–	–	
E1	FORCE_RECOV#	Force Recovery strap pin	Input	CMOS – 1.8V	ST
E2	SLEEP#	Sleep Request to the module from the carrier board. A pull-up is present on the module.	Input	CMOS – 1.8V	ST
E3	SPI0_CLK	SPI 0 Clock	Bidir	CMOS – 1.8V	LV_CZ
E4	SPI0_MISO	SPI 0 MISO	Bidir	CMOS – 1.8V	LV_CZ
E5	I2S3_SDIN	I2S Audio Port 3 Data In	Input	CMOS – 1.8V	ST
E6	I2S3_CLK	I2S Audio Port 3 Clock	Bidir	CMOS – 1.8V	ST
E7	CAM2_MCLK	Camera #2 Master Clock	Output	CMOS – 1.8V	ST
E8	CAM_VSYNC	Camera Vertical Sync	Output	CMOS – 1.8V	ST
E9	UART1_RTS#	UART 1 Request to Send	Output	CMOS – 1.8V	ST
E10	UART1_CTS#	UART 1 Clear to Send	Input	CMOS – 1.8V	ST
E11	RSVD	Not used	–	–	
E12	RSVD	Not used	–	–	
E13	RSVD	Not used	–	–	
E14	SPI1_CS0#	SPI 1 Chip Select 0	Bidir	CMOS – 1.8V	LV_CZ
E15	I2C_GP0_CLK	General I2C Bus #0 Clock	Bidir	Open Drain – 1.8V	DD
E16	AO_DMIC_IN_CLK	Digital Mic Input Clock	Output	CMOS – 1.8V	CZ
E17	RSVD	Not used	–	–	
E18	CAN0_ERR	CAN #0 Error	Input	CMOS – 3.3V	CZ
E19	GND	GND	–	GND	
E20	CSI5_D1–	Camera, CSI 5 Data 1–	Input	MIPI D-PHY	
E21	CSI5_D1+	Camera, CSI 5 Data 1+	Input	MIPI D-PHY	
E22	GND	GND	–	GND	

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
E23	CSI3_D1–	Camera, CSI 3 Data 1–	Input	MIPI D-PHY	
E24	CSI3_D1+	Camera, CSI 3 Data 1+	Input	MIPI D-PHY	
E25	GND	GND	–	GND	
E26	CSI1_D1–	Camera, CSI 1 Data 1–	Input	MIPI D-PHY	
E27	CSI1_D1+	Camera, CSI 1 Data 1+	Input	MIPI D-PHY	
E28	GND	GND	–	GND	
E29	DSI3_D1+	Display, DSI 3 Data 1+	Output	MIPI D-PHY	
E30	DSI3_D1–	Display, DSI 3 Data 1-	Output	MIPI D-PHY	
E31	GND	GND	–	GND	
E32	DSI1_D1+	Display, DSI 1 Data 1+	Output	MIPI D-PHY	
E33	DSI1_D1–	Display, DSI 1 Data 1–	Output	MIPI D-PHY	
E34	GND	GND	–	GND	
E35	DP1_TX3–	DisplayPort 1 Lane 3– / HDMI Clk Lane–	Output	AC-Coupled on carrier board	
E36	DP1_TX3+	DisplayPort 1 Lane 3+ / HDMI Clk Lane+	Output	AC-Coupled on carrier board	
E37	GND	GND	–	GND	
E38	DP1_TX0–	DisplayPort 1 Lane 0– / HDMI Lane 2–	Output	AC-Coupled on carrier board	
E39	DP1_TX0+	DisplayPort 1 Lane 0+ / HDMI Lane 2+	Output	AC-Coupled on carrier board	
E40	GND	GND	–	GND	
E41	PEX1_TX+	PCIe 1 Transmit+ (PCIe #2 Lane 0 muxed w/USB 3.0 port #0)	Output	PCIe PHY, AC-Coupled on carrier board	
E42	PEX1_TX–	PCIe 1 Transmit- (PCIe #2 Lane 0 muxed w/USB 3.0 port #0)	Output	PCIe PHY, AC-Coupled on carrier board	
E43	GND	GND	–	GND	
E44	PEX0_TX+	PCIe #0 Lane 0 Transmit+	Output	PCIe PHY, AC-Coupled on carrier board	
E45	PEX0_TX–	PCIe #0 Lane 0 Transmit–	Output	PCIe PHY, AC-Coupled on carrier board	
E46	GND	GND	–	GND	
E47	GBE_LINK_ACT#	GbE RJ45 connector Link ACT LED0	Output	CMOS – 3.3V tolerant	
E48	GBE_MDI0+	GbE Transformer Data 0+	Bidir	MDI	
E49	GBE_MDI0–	GbE Transformer Data 0–	Bidir	MDI	
E50	PEX1_RST#	PCIe #1 Reset	Output	Open Drain 3.3V, Pull-up on the module	DD
F1	AUDIO_MCLK	Audio Codec Master Clock	Output	CMOS – 1.8V	ST
F2	GPIO19_AUD_RST	Audio Codec Reset or GPIO	Output	CMOS – 1.8V	ST
F3	SPI0_CS0#	SPI 0 Chip Select 0	Bidir	CMOS – 1.8V	ST
F4	SPI0_MOSI	SPI 0 MOSI	Bidir	CMOS – 1.8V	ST
F5	I2S3_LRCLK	I2S Audio Port 3 Left/Right Clock	Bidir	CMOS – 1.8V	ST
F6	I2S3_SDOUT	I2S Audio Port 3 Data Out	Bidir	CMOS – 1.8V	ST

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
F7	GPIO1_CAM1_PWR#	Camera 1 Powerdown or GPIO	Output	CMOS – 1.8V	ST
F8	CAM1_MCLK	Camera 1 Reference Clock	Output	CMOS – 1.8V	ST
F9	CAM0_MCLK	Camera 0 Reference Clock	Output	CMOS – 1.8V	ST
F10	GND	GND	–	GND	
F11	RSVD	Not used	–	–	
F12	RSVD	Not used	–	–	
F13	SPI1_MOSI	SPI 1 MOSI	Bidir	CMOS – 1.8V	ST
F14	SPI1_MISO	SPI 1 MISO	Bidir	CMOS – 1.8V	ST
F15	GND	GND	–	GND	
F16	SPI2_CS1#	SPI 2 Chip Select 1	Bidir	CMOS – 1.8V	ST
F17	SDCARD_CD#	SD Card Card Detect	Input	CMOS – 1.8V	ST
F18	SDCARD_D3	SD Card / SDIO Data 3	Bidir	CMOS – 3.3/1.8V	CZ
F19	SDCARD_D2	SD Card / SDIO Data 2	Bidir	CMOS – 3.3/1.8V	CZ
F20	SDCARD_WP	SD Card Write Protect	Input	CMOS – 1.8V	ST
F21	GND	GND	–	GND	
F22	CSI4_D0–	Camera, CSI 4 Data 0–	Input	MIPI D-PHY	
F23	CSI4_D0+	Camera, CSI 4 Data 0+	Input	MIPI D-PHY	
F24	GND	GND	–	GND	
F25	CSI2_D0–	Camera, CSI 2 Data 0–	Input	MIPI D-PHY	
F26	CSI2_D0+	Camera, CSI 2 Data 0+	Input	MIPI D-PHY	
F27	GND	GND	–	GND	
F28	CSI0_D0–	Camera, CSI 0 Data 0–	Input	MIPI D-PHY	
F29	CSI0_D0+	Camera, CSI 0 Data 0+	Input	MIPI D-PHY	
F30	GND	GND	–	GND	
F31	DSI2_D0+	Display, DSI 2 Data 0+	Output	MIPI D-PHY	
F32	DSI2_D0–	Display, DSI 2 Data 0–	Output	MIPI D-PHY	
F33	GND	GND	–	GND	
F34	DSI0_D0+	Display, DSI 0 Data 0+	Output	MIPI D-PHY	
F35	DSI0_D0–	Display, DSI 0 Data 0–	Output	MIPI D-PHY	
F36	GND	GND	–	GND	
F37	DP0_TX1–	DisplayPort 0 Lane 1– / HDMI Lane 1–	Output	AC-Coupled on carrier board	
F38	DP0_TX1+	DisplayPort 0 Lane 1+ / HDMI Lane 1+	Output	AC-Coupled on carrier board	
F39	GND	GND	–	GND	
F40	PEX2_RX+	PCIe #0 Lane 2/PCIE #1 Lane 0 Receive+	Input	PCIe PHY, AC-Coupled on carrier board	
F41	PEX2_RX–	PCIe #0 Lane 2/PCIE #1 Lane 0 Receive–	Input	PCIe PHY, AC-Coupled on carrier board	

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
F42	GND	GND	–	GND	
F43	USB_SS0_RX+	USB 3.0 #1 Receive+ (muxed w/PEX1)	Input	USB SS PHY, AC-Coupled (off the module)	
F44	USB_SS0_RX–	USB 3.0 #1 Receive– (muxed w/PEX1)	Input	USB SS PHY, AC-Coupled (off the module)	
F45	GND	GND	–	GND	
F46	GBE_LINK1000#	GbE RJ45 connector Link 1000 LED2	Output	CMOS – 3.3V Tolerant	
F47	GBE_MDI1+	GbE Transformer Data 1+	Bidir	MDI	
F48	GBE_MDI1–	GbE Transformer Data 1–	Bidir	MDI	
F49	GND	GND	–	GND	
F50	GBE_LINK100#	GbE RJ45 connector Link 100 LED1	Output	CMOS – 3.3V Tolerant	
G1	I2S0_SDIN	I2S Audio Port 0 Data In	Input	CMOS – 1.8V	ST
G2	I2S0_CLK	I2S Audio Port 0 Clock	Bidir	CMOS – 1.8V	ST
G3	GND	GND	–	GND	
G4	DSPK_OUT_CLK	Digital Speaker Output Clock	Output	CMOS – 1.8V	ST
G5	I2S2_CLK	I2S Audio Port 2 Clock	Bidir	CMOS – 1.8V	ST
G6	I2S2_SDIN	I2S Audio Port 2 Data In	Input	CMOS – 1.8V	ST
G7	GPIO4_CAM_STROBE	Camera Strobe or GPIO	Output	CMOS – 1.8V	ST
G8	GPIO0_CAM0_PWR#	Camera 0 Powerdown or GPIO	Output	CMOS – 1.8V	ST
G9	UART3_CTS#	UART 3 Clear to Send	Input	CMOS – 1.8V	ST
G10	UART3_RTS#	UART 3 Request to Send	Output	CMOS – 1.8V	ST
G11	UART0_RTS#	UART 0 Request to Send	Output	CMOS – 1.8V	ST
G12	UART0_RX	UART 0 Receive	Input	CMOS – 1.8V	ST
G13	SPI1_CLK	SPI 1 Clock	Bidir	CMOS – 1.8V	ST
G14	GPIO9_MOTION_INT	Motion Interrupt or GPIO	Input	CMOS – 1.8V	ST
G15	SPI2_MOSI	SPI 2 MOSI	Bidir	CMOS – 1.8V	ST
G16	SPI2_CS0#	SPI 2 Chip Select 0	Bidir	CMOS – 1.8V	ST
G17	GND	GND	–	GND	
G18	SDCARD_CLK	SD Card / SDIO Clock	Output	CMOS – 3.3/1.8V	CZ
G19	SDCARD_CMD	SD Card / SDIO Command	Bidir	CMOS – 3.3/1.8V	CZ
G20	GND	GND	–	GND	
G21	CSI4_CLK–	Camera, CSI 4 Clock–	Input	MIPI D-PHY	
G22	CSI4_CLK+	Camera CSI 4 Clock+	Input	MIPI D-PHY	
G23	GND	GND	–	GND	
G24	CSI2_CLK–	Camera, CSI 2 Clock–	Input	MIPI D-PHY	
G25	CSI2_CLK+	Camera, CSI 2 Clock+	Input	MIPI D-PHY	
G26	GND	GND	–	GND	
G27	CSI0_CLK–	Camera, CSI 0 Clock–	Input	MIPI D-PHY	

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
G28	CSI0_CLK+	Camera, CSI 0 Clock+	Input	MIPI D-PHY	
G29	GND	GND	–	GND	
G30	DSI2_CLK+	Display DSI 2 Clock+	Output	MIPI D-PHY	
G31	DSI2_CLK–	Display DSI 2 Clock–	Output	MIPI D-PHY	
G32	GND	GND	–	GND	
G33	DSI0_CLK+	Display, DSI 0 Clock+	Output	MIPI D-PHY	
G34	DSI0_CLK–	Display, DSI 0 Clock–	Output	MIPI D-PHY	
G35	GND	GND	–	GND	
G36	DP0_TX2–	DisplayPort 0 Lane 2– / HDMI Lane 0–	Output	AC-Coupled on carrier board	
G37	DP0_TX2+	DisplayPort 0 Lane 2+ / HDMI Lane 0+	Output	AC-Coupled on carrier board	
G38	GND	GND	–	GND	
G39	PEX_RFU_RX+	PCIe #0 Lane 3 or USB_SS#1 Receive+	Input	PCIe PHY, AC-Coupled on carrier board	
G40	PEX_RFU_RX–	PCIe #0 Lane 3 or USB_SS#1 Receive–	Input	PCIe PHY, AC-Coupled on carrier board	
G41	GND	GND	–	GND	
G42	USB_SS1_RX+	PCIe #0 Lane 1 or USB 3.0 #2 Receive+	Input	USB SS PHY, AC-Coupled (off the module)	
G43	USB_SS1_RX–	PCIe #0 Lane 1 or USB 3.0 #2 Receive–	Input	USB SS PHY, AC-Coupled (off the module)	
G44	GND	GND	–	GND	
G45	SATA_RX+	SATA Receive+	Input	SATA PHY, AC-Coupled on carrier board	
G46	SATA_RX–	SATA Receive–	Input	SATA PHY, AC-Coupled on carrier board	
G47	GND	GND	–	GND	
G48	GBE_MDI2+	GbE Transformer Data 2+	Bidir	MDI	
G49	GBE_MDI2–	GbE Transformer Data 2–	Bidir	MDI	
G50	GND	GND	–	GND	
H1	I2S0_LRCLK	I2S Audio Port 0 Left/Right Clock	Bidir	CMOS – 1.8V	ST
H2	I2S0_SDOUT	I2S Audio Port 0 Data Out	Bidir	CMOS – 1.8V	ST
H3	GPIO20_AUD_INT	Audio Codec Interrupt or GPIO	Input	CMOS – 1.8V	ST
H4	DSPK_OUT_DAT	Digital Speaker Output Data	Output	CMOS – 1.8V	ST
H5	I2S2_LRCLK	I2S Audio Port 2 Left/Right Clock	Bidir	CMOS – 1.8V	ST
H6	I2S2_SDOUT	I2S Audio Port 2 Data Out	Bidir	CMOS – 1.8V	ST
H7	GPIO3_CAM1_RST#	Camera 1 Reset or GPIO	Output	CMOS – 1.8V	ST
H8	GPIO2_CAM0_RST#	Camera 0 Reset or GPIO	Output	CMOS – 1.8V	ST
H9	UART3_RX	UART 3 Receive	Input	CMOS – 1.8V	ST
H10	UART3_TX	UART 3 Transmit	Output	CMOS – 1.8V	ST
H11	UART0_CTS#	UART 0 Clear to Send	Input	CMOS – 1.8V	ST

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
H12	UART0_TX	UART 0 Transmit	Output	CMOS – 1.8V	ST
H13	GPIO8_ALS_PROX_INT	Proximity sensor Interrupt or GPIO	Input	CMOS – 1.8V	ST
H14	SPI2_CLK	SPI 2 Clock	Bidir	CMOS – 1.8V	ST
H15	SPI2_MISO	SPI 2 MISO	Bidir	CMOS – 1.8V	ST
H16	SDCARD_PWR_EN	SD Card power switch Enable	Output	CMOS – 1.8V	ST
H17	SDCARD_D1	SD Card / SDIO Data 1	Bidir	CMOS – 3.3V/1.8V	CZ
H18	SDCARD_D0	SD Card / SDIO Data 0	Bidir	CMOS – 3.3V/1.8V	CZ
H19	GND	GND	–	GND	
H20	CSI4_D1–	Camera, CSI 4 Data 1–	Input	MIPI D-PHY	
H21	CSI4_D1+	Camera, CSI 4 Data 1+	Input	MIPI D-PHY	
H22	GND	GND	–	GND	
H23	CSI2_D1–	Camera, CSI 2 Data 1–	Input	MIPI D-PHY	
H24	CSI2_D1+	Camera, CSI 2 Data 1+	Input	MIPI D-PHY	
H25	GND	GND	–	GND	
H26	CSI0_D1–	Camera, CSI 0 Data 1–	Input	MIPI D-PHY	
H27	CSI0_D1+	Camera, CSI 0 Data 1+	Input	MIPI D-PHY	
H28	GND	GND	–	GND	
H29	DSI2_D1+	Display, DSI 2 Data 1+	Output	MIPI D-PHY	
H30	DSI2_D1–	Display, DSI 2 Data 1–	Output	MIPI D-PHY	
H31	GND	GND	–	GND	
H32	DSI0_D1+	Display, DSI 0 Data 1+	Output	MIPI D-PHY	
H33	DSI0_D1–	Display, DSI 0 Data 1–	Output	MIPI D-PHY	
H34	GND	GND	–	GND	
H35	DP0_TX3–	DisplayPort 0 Lane 3– / HDMI Clk Lane–	Output	AC-Coupled on carrier board	
H36	DP0_TX3+	DisplayPort 0 Lane 3+ / HDMI Clk Lane+	Output	AC-Coupled on carrier board	
H37	GND	GND	–	GND	
H38	DP0_TX0–	DisplayPort 0 Lane 0– / HDMI Lane 2–	Output	AC-Coupled on carrier board	
H39	DP0_TX0+	DisplayPort 0 Lane 0+ / HDMI Lane 2+	Output	AC-Coupled on carrier board	
H40	GND	GND	–	GND	
H41	PEX1_RX+	PCIe #2 Lane 0 Receive+ (muxed w/USB_SS#0)	Input	PCIe PHY, AC-Coupled on carrier board	
H42	PEX1_RX–	PCIe #2 Lane 0 Receive– (muxed w/USB_SS#0)	Input	PCIe PHY, AC-Coupled on carrier board	
H43	GND	GND	–	GND	
H44	PEX0_RX+	PCIe #0 Lane 0 Receive+	Input	PCIe PHY, AC-Coupled on carrier board	
H45	PEX0_RX–	PCIe #0 Lane 0 Receive–	Input	PCIe PHY, AC-Coupled on carrier board	

Pin #	Module Pin Name	Usage/Description	Direction	Pin Type	MPIO Type
H46	GND	GND	–	GND	
H47	GBE_MDI3+	GbE Transformer Data 3+	Bidir	MDI	
H48	GBE_MDI3–	GbE Transformer Data 3–	Bidir	MDI	
H49	GND	GND	–	GND	
H50	RSVD	Not used	–	–	

6.0 Physical / Electrical Characteristics

6.1 Absolute Maximum Ratings

The absolute maximum ratings describe stress conditions. These parameters do not set minimum and maximum operating conditions that will be tolerated over extended periods of time. If the device is exposed to these parameters for extended periods of time, no guarantee is made and device reliability may be affected. It is not recommended to operate a Jetson TX2 series module under these conditions, recommended operating conditions are provided in the following section.

WARNING: Exceeding the listed conditions may damage and/or affect long-term reliability of the part.
The Jetson TX2 series module should never be subjected to conditions exceeding absolute maximum ratings.

Table 58 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
VDD_{MAX}	VDD_IN	-0.5	22.5	V	
	VDD_RTC	-0.3	6.0	V	
IDD_{MAX}	VDD_IN Imax		3	A	Software limited. 3A is for VDD_{MAX}(19V). Actual IDD_{MAX} is dependent on VDD_IN (VDD_IN_{MIN})
V_{M_PIN}	Voltage applied to any powered I/O pin	-0.5	VDD + 0.5	V	
	DD pads configured as open drain	-0.5	3.63	V	pad's output-driver must be set to open-drain mode
T_{TTP}	Operating Temperature: measured on Thermal Transfer Plate	-25	80	°C	TX2
		-40	85	°C	TX2i
T_{STG}	Storage Temperature	-25	80	°C	TX2
		-40	85	°C	TX2i

6.2 Recommended Operating Conditions

The parameters listed in following table are specific to a temperature range and operating voltage. Operating a Jetson TX2 series module beyond these parameters is not recommended. Exceeding these conditions for extended periods may adversely affect device reliability.

Table 59 Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD_{DC}	VDD_IN	5.5 (‡)		19.6	V	**TX2** – (‡) 5.75V with OC1 throttling (throttlectl_oc1) enabled
		9.0		19.0	V	**TX2i**
	VDD_RTC	1.65		5.5	V	**TX2 / TX2i**

NOTE: Hardware throttling is used to respond to transient electrical and thermal events (e.g., Over-current, voltage droop, temperature spikes). Throttling may cause lower performance; however, since these events are rare and transient in nature, the user experience is minimally impacted. Firmware refers to these as OC alarms and triggers.

- The trigger point for a voltage droop event when using a battery is below 5.75V (OC1 throttling enabled); for system using AC adaptor the trigger point for a voltage droop event is below 5.5V (OC1 throttling disabled).
- When used with a 2 cell battery, throttling is not required but strongly recommended; OC1 throttling setting is modified when flashing system (see the *Platform Adaptation and Bring-up Guide* for information on flashing your system).
- A supply voltage (VDD_IN) not less than 6V should be used when flashing the module.

6.3 Digital Logic

Voltages less than the minimum stated value can be interpreted as an undefined state or logic level low which may result in unreliable operation. Voltages exceeding the maximum value can damage and/or adversely affect device reliability.

Table 60. CMOS Pad Type DC Characteristics

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.70 x VDD	0.5 + VDD	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.75 x VDD	---	V

Table 61 Open Drain Pad Type DC Characteristics

Symbol	Description	Min	Max	Units
V_{IL}	Input Low Voltage	-0.5	0.25 x VDD	V
V_{IH}	Input High Voltage	0.75 x VDD	3.63	V
V_{OL}	Output Low Voltage (I_{OL} = 1mA)	---	0.15 x VDD	V
V_{OH}	Output High Voltage (I_{OH} = -1mA)	0.85 x VDD	---	V

6.4 Environmental & Mechanical Screening (TX2 only)

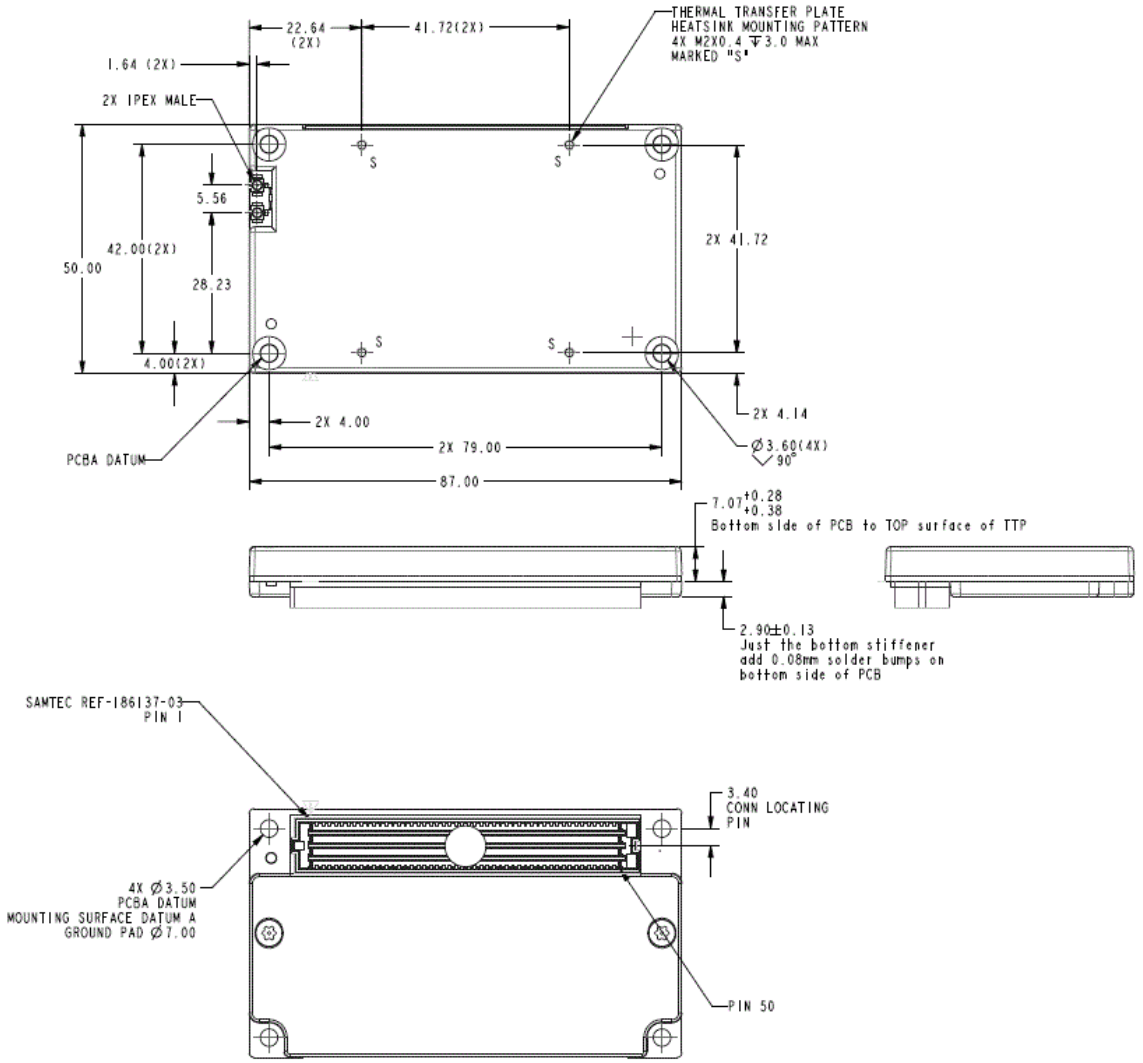
Jetson TX2 module performance was assessed against a series of industry standard tests designed to evaluate robustness and estimate the failure rate of an electronic assembly in the environment in which it will be used. Mean Time Between Failures (MTBF) calculations are produced in the design phase to predict a product's future reliability in the field.

Table 62 Reliability Tests and Standards

Test	Reference Standard	Notes
Temperature Humidity	JESD22-A101	Pass
System Level Power Cycling	JESD22-A122	Pass
Board Level Temperature Cycling	JESD22-A104, IPC9701	Pass
Mechanical Shock	JESD22B110	Pass
Bending	IPC9702	Pass
Connector Insertion	EIA-364	Pass
Random Vibration	JEDEC22-B103B	Pass
Low/High Temp Boot	NV – Standard	Pass
Damp Heat Cycle	IEC 60068-2-30	Pass
Thermal Shock	IEC 60068-2-14	Pass
MTBF/Failure Rate Controlled Environment (GB)	Telcordia SR-332; Issue 3	2,278K Hrs / 439 FIT
MTBF/Failure Rate Uncontrolled Environment (GF)	Telcordia SR-332; Issue 3	1,139K Hrs / 878 FIT

6.5 Package Drawings and Dimensions

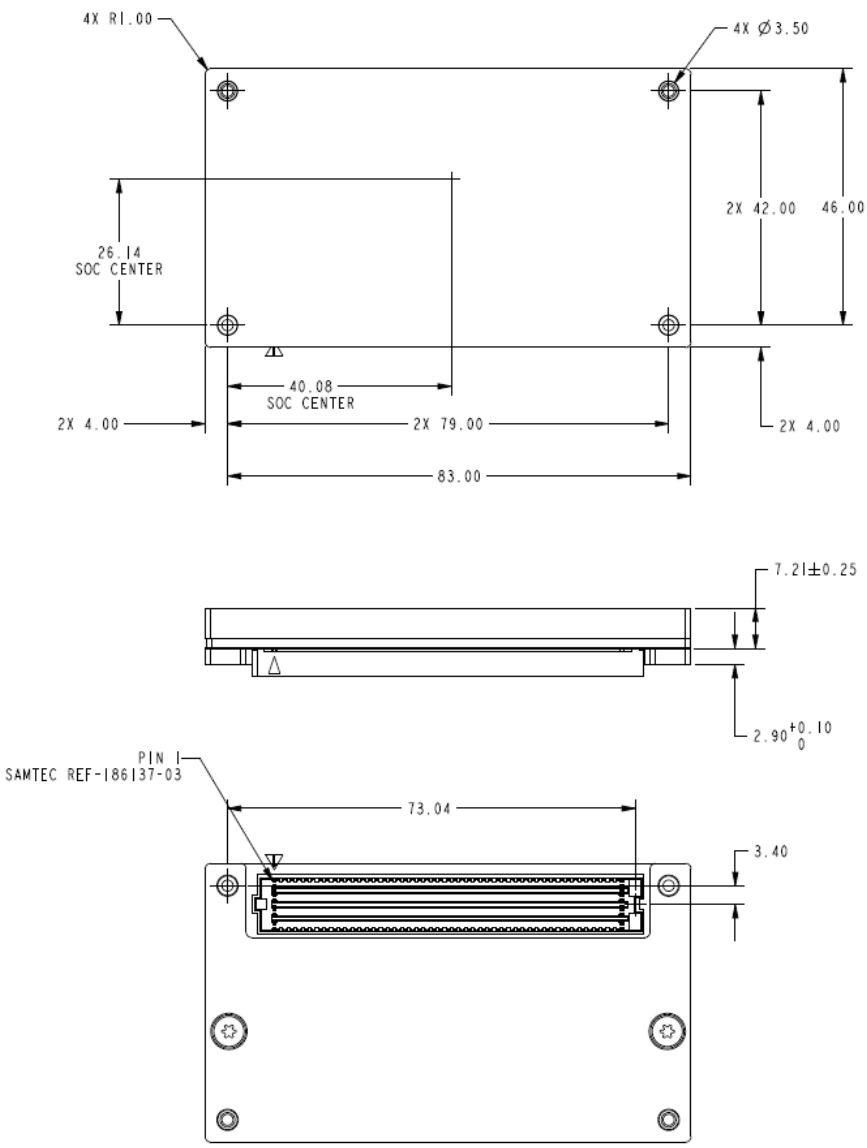
Figure 7 TX2 SOM Package Outline with Dimensions



NOTES

- Carrier Board connector location & mounting holes should match the Jetson TX2 module dimensions shown in figure above.
- Carrier Board components limited to 2.5mm under outline of the Jetson TX2i module. This assumes the use of A SEARAY mating connector, “SAMTEC REF-186138-02” (SEAM-50-02.0-S-08-2-A-K-TR) or Molex receptacle (PN:45970-001). If the connector used is taller, the max component height may change accordingly.
- Keepout area on Carrier Board for standoffs depends on diameter of standoffs used. The Jetson TX2 module carrier board uses 6MM diameter round keepout areas surrounding the four mounting holes. These areas on the PCB should be GND with no soldermask. See the Jetson TX2 Carrier Board layout for reference.
- All dimensions are in millimeters unless otherwise specified.
- Tolerances are: .X ± 0.25, .XX ± 0.10, Angles ± 1°
- Mass: 88 ±1.7% Grams
- Thermal transfer plate and bottom stiffener finish: Clear Chemfilm per MIL-C-5541-E Class 3

Figure 8 TX2i SOM Package Outline with Dimensions

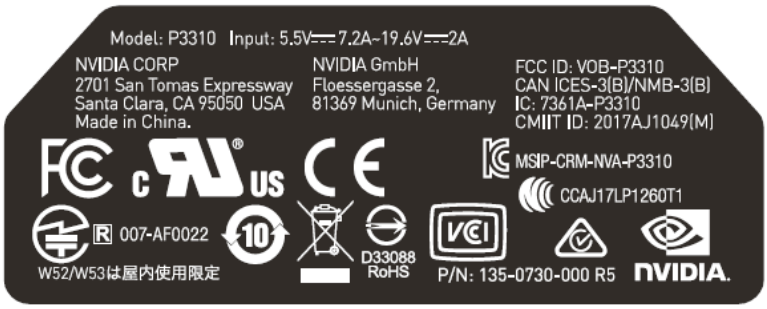


NOTES

- Carrier Board connector location & mounting holes should match the Jetson TX2i module dimensions shown in figure above.
- Carrier Board components limited to 2.5mm under outline of the Jetson TX2i module. This assumes the use of A SEARAY mating connector, “SAMTEC REF-186138-02” (SEAM-50-02.0-S-08-2-A-K-TR) or Molex receptacle (PN:45970-001). If the connector used is taller, the max component height may change accordingly.
- Keepout area on Carrier Board for standoffs depends on diameter of standoffs used. The Jetson TX2i module carrier board uses 6MM diameter round keepout areas surrounding the four mounting holes. These areas on the PCB should be GND with no soldermask. See the Jetson TX2i Carrier Board layout for reference.
- All dimensions are in millimeters unless otherwise specified.
- Tolerances are: .X ± 0.30, .XX ± 0.20, Angles ± 1°
- Mass: 99 ±2% Grams
- Thermal transfer plate and bottom stiffener finish: Clear Chemfilm per MIL-C-5541-E Class 3

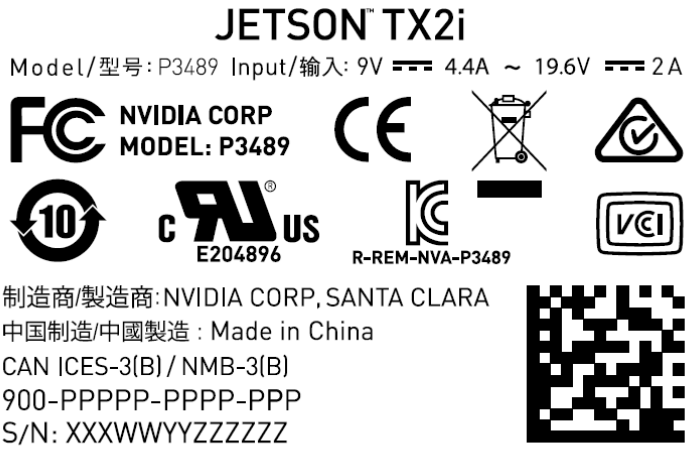
6.6 Module Marking

Figure 9 TX2 SOM Marking (Black Label)



* Device SN and MAC Address information located on individual labels applied to sides of module.

Figure 10 TX2i SOM Marking (Laser Etching)



* ECC 200 Barcode: Contains Device SN and MAC1 Address (e.g., 0424617123456,00044BA4F228 – there is no space between SN and MAC1, only a comma)

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