PCIe-DIO-48JPS, PCIe-DIO-48JPLS
PCIe-DIO-48JP, PCIe-DIO-48JPL

PCI Express Digital I/O w/Change of State Detection

FEATURES

- 48 channel high-current TTL digital I/O lines
- Change of State (COS) detection and interrupt capabilities
- Compatible with industry standard 8255 PPI
- 68-pin SCSI pin-in-socket female connector on card mounting bracket
- User interrupt pin
- All 48 digital I/O lines buffered with 32mA source / 64mA sink current capabilities
- Four and eight bit ports independently selectable for inputs or outputs
- Jumper configurable pull-up/-down on DIO lines
- 5V VCCIO (3.3V jumper configurable)
- Fused VCCIO available on I/O connector

FACTORY OPTIONS

- Extended temperature operation (-40° to +85°C)
- 48 channel card without change of state feature

FUNCTIONAL DESCRIPTION

The PCIe-DIO-48JPS is a 48 channel PCI Express (PCIe) card designed for use in a variety of digital I/O applications. It uses the high speed PCI Express bus to transfer digital data to and from the card. The digital I/O is compatible with 8255 PPI chips making it easy to program. This also allows for simple and trouble-free migration from other ACCES PCI digital I/O cards . The card features a x1 lane PCI Express connector which can be used in any available x1, x2, x4, x8, x12, or x16 PCI Express expansion slot. The card is 6.6 inches in length and 4.2 inches seated height.

Two 24 line groups each have three 8-bit I/O ports designated A, B and C. Port C can be further divided into two 4-bit nybbles. Each port can be programmed as inputs or outputs. Change of State (COS) detection and interrupt capabilities are designed to relieve software from polling routines that can consume valuable processing time. Each port can be programmed for detecting state changes on their lines, in which any changes of the enabled port's bits (low-to-high or high-to-low) will generate an IRQ. An ISR (interrupt service routine) then polls the port to determine which bit changed state and clear the interrupt.

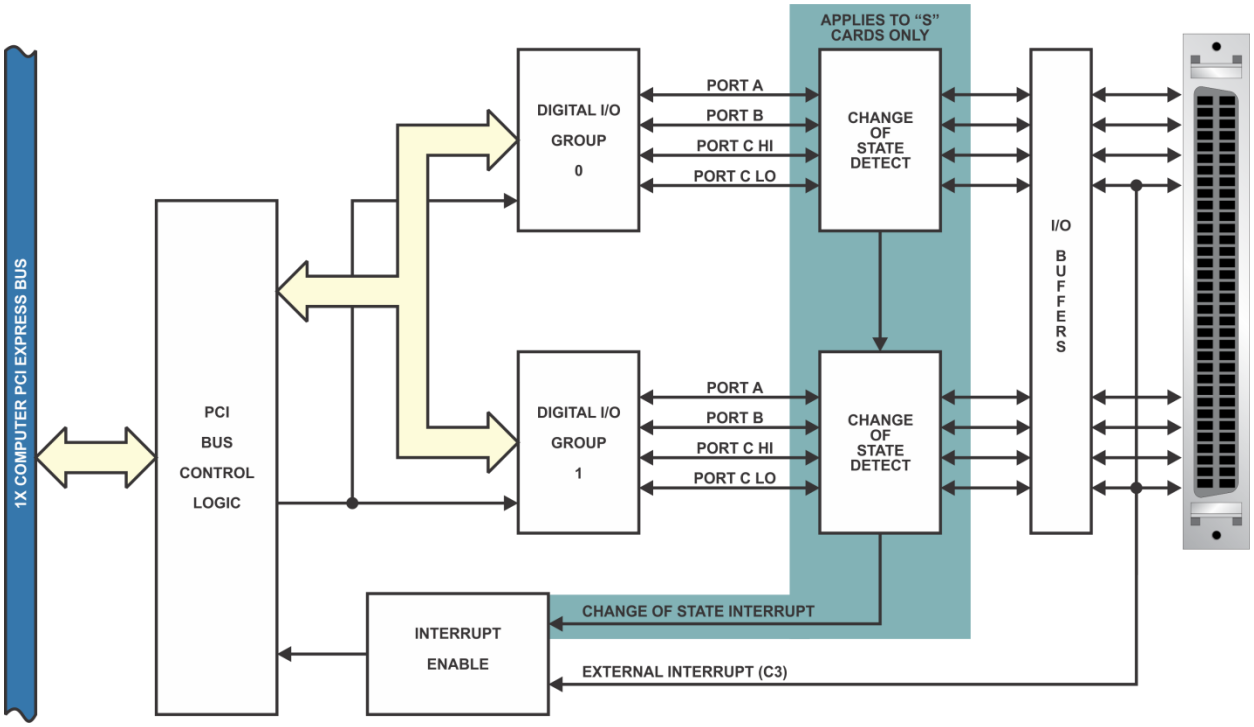
This card is an excellent choice for system designs that would benefit from using a wiring harness to connect up to a complete system. This is due to the 68-pin I/O connector being located on the card mounting bracket, it is a much cleaner card solution to use compared to routing ribbon cables through a cutout on the card mounting bracket, then plugging them onto the headers on the side of the card.

ACCESSORIES

Available accessories include ribbon cables and shielded round-wire molded cable assemblies. Screw terminal boards and DIN-rail mounts are also available for a variety of quick and easy connectivity options.

SOFTWARE

The card is supported for use in most operating systems and includes Linux and Windows compatible software packages. This package contains sample programs and source code in Delphi and Visual C++ for Windows. Linux support includes installation files and basic samples for programming from user level via an open source kernel driver. Third party support includes a Windows standard DLL interface usable from the most popular application programs. Embedded OS support includes Windows.



BLOCK DIAGRAM

SPECIFICATIONS

VCCIO	5V (TTL) or 3.3V (LVTTL)
Digital Inputs	
Logic High	2.0V to VCCIO
Logic Low	0V to 0.8V
Current	±20uA (max)
Digital Outputs	
Logic High	2.0V (min); 32mA source
Logic Low	0.55V (max); 64mA sink
Power Output	VCCIO via 0.5A resettable fuse
Environmental	
Operating Temperature	0° to 70°C, optional -40° to +85°C
Storage Temperature	-55° to +150°C
Humidity	5% to 95% RH, w/o condensation
Card Dimensions	Length - 6.6"; Height - 4.2" (seated)
I/O Connector	TE Receptacle Assy, .050 Series, Amplimite P/N 1761028-4

ORDERING GUIDE

- PCIe-DIO-48JPLS — DIO w/ COS & latching connector
- PCIe-DIO-48JPS — DIO w/ COS & screwlocks
- PCIe-DIO-48JPL — DIO w/ latching connector
- PCIe-DIO-48JP — DIO w/ screwlocks

Factory Options

- Extended temperature operation (-40° to +85°C)

Optional Accessories

- C68PS18L — Shielded latching cable, 18"
- CAB68-36L — Shielded latching cable, 36"
- STB-68 — Screw term bd w/conn. latches
- CAB68-36J — Shielded jackscrew cable, 36"
- STB-68-S01 — Screw term bd w/conn. screwlocks

68-Position Connector Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	Group 0 Port C Hi PC7	35	Ground
2	Group 0 Port C Hi PC6	36	Ground
3	Group 0 Port C Hi PC5	37	Group 1 Port C Hi PC7
4	Group 0 Port C Hi PC4	38	Group 1 Port C Hi PC6
5	Group 0 Port C Lo PC3*	39	Group 1 Port C Hi PC5
6	Group 0 Port C Lo PC2	40	Group 1 Port C Hi PC4
7	Group 0 Port C Lo PC1	41	Group 1 Port C Lo PC3*
8	Group 0 Port C Lo PC0	42	Group 1 Port C Lo PC2
9	Ground	43	Group 1 Port C Lo PC1
10	Ground	44	Group 1 Port C Lo PC0
11	Ground	45	Ground
12	Ground	46	Ground
13	Group 0 Port B PB7	47	Ground
14	Group 0 Port B PB6	48	Ground
15	Group 0 Port B PB5	49	Group 1 Port B PB7
16	Group 0 Port B PB4	50	Group 1 Port B PB6
17	Group 0 Port B PB3	51	Group 1 Port B PB5
18	Group 0 Port B PB2	52	Group 1 Port B PB4
19	Group 0 Port B PB1	53	Group 1 Port B PB3
20	Group 0 Port B PB0	54	Group 1 Port B PB2
21	Ground	55	Group 1 Port B PB1
22	Ground	56	Group 1 Port B PB0
23	Ground	57	Ground
24	Ground	58	Ground
25	Group 0 Port A PA7	59	Group 1 Port A PA7
26	Group 0 Port A PA6	60	Group 1 Port A PA6
27	Group 0 Port A PA5	61	Group 1 Port A PA5
28	Group 0 Port A PA4	62	Group 1 Port A PA4
29	Group 0 Port A PA3	63	Group 1 Port A PA3
30	Group 0 Port A PA2	64	Group 1 Port A PA2
31	Group 0 Port A PA1	65	Group 1 Port A PA1
32	Group 0 Port A PA0	66	Group 1 Port A PA0
33	Ground	67	Fused VCCIO**
34	Ground	68	Fused VCCIO**

* PC3 is an I/O pin and also a user interrupt
** VCCIO is protected by a resettable 0.5A fuse

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